Please report comments to sc99proceedings@sc99.org

Message from the Conference Chair:

Welcome to the Proceedings for SC99! Let me tell you a little about our plans for the conference...

Extended Conference Theme

Our focus will be the remarkable impact that high-end technology has had on the rest of the computing world. The most obvious influence of high-end technology is its impressive trickle-down effect. Innovations in architecture performance, wide-area networking, visualization, and high volume storage have all been driven by needs at the high-end. Within a remarkably short time those innovations have permeated into mainstream computing technology. HPC may represent a relatively small portion of the overall computing marketplace, but it certainly is a driving force for innovation and change.

At SC99, invited speakers and special sessions will address the issues of trickle-down. Is it happening fast enough? Do we need to develop more deliberate strategies for technology transfer? What societal obligations are associated with technological innovation, and who should assume responsibility for them? These sessions will augment the late-breaking research contributions that will make up the technical paper sessions.

SC99 will also explore how numerical modeling and simulation techniques developed for high-end applications have transformed industrial R&D. In addition to our research exhibits and industry exhibits, we'll host a new series of special exhibits that demonstrate how HPC techniques have been used to reduce both time-to-market and bottom-line costs with examples as diverse as motorcycle helmets, cancer drugs, stereo speakers, and the gaming industry.

One-of-a-kind Networking Infrastructure

Our conference network, SCinet99, will showcase the newest aspect of networking: networks that are no longer captives of voice-based infrastructure. For too long, our wide-area networks have had to rely on technologies that were designed to support voice transmissions, not digital traffic. SC99 will roll out the network technologies of the future.

For connections to the world, SC99 will enjoy full OC-192 connectivity, with multiple, highspeed cross-connects to Abilene, DREN, the vBNS, ESnet -- or whatever your favorite backbone is. Exhibitors will have the chance to show the potential impact of a full-scale, ultra-high-speed information infrastructure. How are we going to do this for SC99? Our initial partners include GST, the National Transparent Optical Network, and US West. By fall of 1999, NTON will deploy a 10Gbs, multiple wavelength network linking Seattle and

San Diego via Portland. GST and US West will connect the convention center to NTON so exhibitors at SC99 can exploit these unique capabilities.

Within the Convention Center, we'll be deploying another exciting new network technology: high-speed free-space optics. For those of you who haven't heard about this, it means that high-performance networking can now be accomplished literally through the air -- without wires or fiber. At SC99, we'll have a free-space optical mesh operating at OC-3 speeds.

Innovative Education Program

The growing availability of affordable HPNC is spurring educators to reconsider the role that technology should play in education, particularly at K-12 levels. SC99's education program will address several key aspects of this problem. For example, should we be placing emphasis on "technology literacy" -- how to learn and use new capabilities? Or should we focus on "technology integration" -- how technology fits into a broader social and business context?

By bringing together scientists, engineers, managers, educators, and researchers from all areas of high-performance technology, SC99 will provide a powerful arena for exploring the theme of how high-end innovations affect the rest of the computing world.

Dispelling Myths about Portland

SC99 will take place in Portland, Oregon. Don't get us confused with Portland, Maine that's on the other side of the country. We're the Portland on the left. This is the first time that SC will return both to a particular city and a particular Convention Center. We were there for SC93, and we're returning because we had such favorable reviews from attendees and exhibitors.

I'd like to take this opportunity to dispel a few myths about Portland.

MYTH #1: Portland is just an average American city

- Not true! Portland has the world's second-largest copper statue (after statue of Liberty) affectionately known as "Queen Kong"
- Portland is the wind-surfing capital of the world. In addition, you'll find year-round skiing about 1 hour to the east, and some of the world's most rugged coastal scenery about an hour to the west.
- If you prefer indoor sports, how about Powell's the country's largest bookstore? And there's no sales tax in Oregon!
- Portland is also the birthplace of the GardenBurger (and would you believe the name of the company that created it is "Wholesome & Hearty"?)

MYTH #2 - Oregonians are health freaks

- Portland has more microbreweries per capita than any other city in world. Also 66% of world's hops are grown within Oregon, so you know the beer is great!
- Portland ties with Seattle for having the most coffee outlets per capita
- There are 462 vineyards in state - 47 wineries within 100 miles of Portland
- We're also probably the only state you know that has an official "state nut." It's the hazelnut; at SC99 we'll be giving out free samples!

MYTH #3 - "... but Portland is rainy..."

- Not true! We have less annual rainfall than Miami, Dallas, or New York. We also have *considerably* less rain than London, Bangkok, or Seattle.
- That means you'll want to enjoy Oregon's incredible outdoor activities. Did you know that 56% of the state of Oregon is publicly owned land? Approximately half of the state is forested, which means we have almost 30 million acres of forests.
- Then there are our extremes: Hell's Canyon is the deepest canyon in the US. Crater Lake is the country's deepest lake. And Multnomah Falls just half an hour from downtown Portland is the second-highest waterfall.

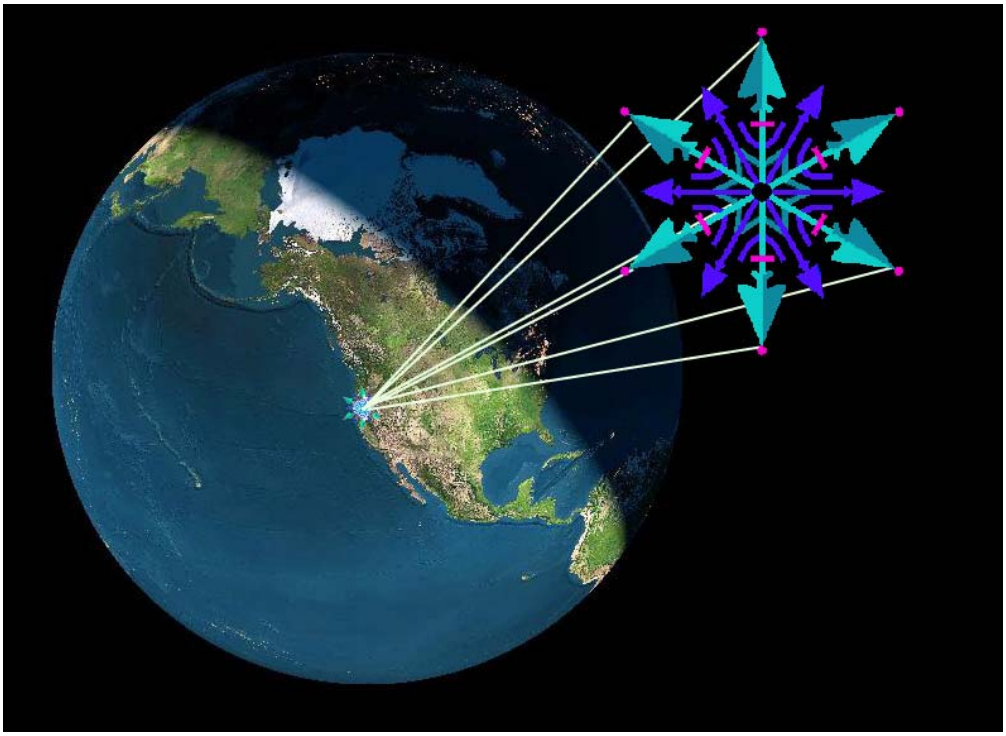
MYTH #4 - Oregon isn't a technology hotspot

- Wrong again! Oregon's #1 industry is high-tech
- You know, few people realize that Oregon serves as the telecommunications gateway to the Pacific, with all major transPacific fiber lines touching land along the Oregon Coast. In fact, whenever you make a phone call to Asia, or send commodity email across the Pacific, chances are your voice or data is passing through Oregon. So in a sense, you've already been to Oregon!

MYTH #5 - Oregon is too far away

- Actually, Oregon is the quintessence of "centrally located". Did you know that Port Orford, OR, is actually the geographic center of the US (if you count Alaska and Hawaii, that is).
- And Portland is just about equidistant from Tokyo and from London.

In case you don't believe me, just check out the latest satellite photos:



I hope you'll give me and the rest of the conference committees a chance to welcome you in Portland this November!

Cherri Pancake, Conference Chair
Oregon State University

pancake@cs.orst.edu

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SC'99

Conference at a Glance

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Tutorials		8:30am - 5pm	8:30am - 5pm
Education Program		8:30am - 7pm	8am - 7pm
Registration & Store	1 - 6pm	7:30am - 6pm	7:30am - 9pm
			Monday, 7 - 9pm **GALA OPENING** Preview all SC99 exhibits!

	TUESDAY	WEDNESDAY	THURSDAY	FRIDAY
Keynote Address	8:30 - 10am **Donna Shirley**			
State-of-the-Field		8am V. Cerf 9am S. Stolfo	8am G. Papadopoulos 9am D. Reed	
Invited Speakers	10:30am D. Crawford 11:15am A. Chien	10:30am M. Ellisman 11:15am C. Johnson	10:30am J. Koza 11:15am T. Sterling	
Technical Sessions Technical Papers Panels	10:30am - noon **PAPERS** **Scientific Applications I** • **Scheduling I** • **Compilers**	10:30am - noon **PAPERS** **Grid Computing** • **Numerical Algorithms II** • **Low-level Architecture**	10:30am - noon **PAPERS** **Message Passing** • **Performance II**	8:30 - 10am **PANELS** **Challenges & Opportunities of the Scalable Information Infrastructure** • **The Role of Java in High Performance Network Computing** • **Bioinformatics and High Performance Computing**
	1:30 - 3pm **PAPERS** **Ocean & Climate Modeling** • **Non-Numeric Algorithms** • **Performance I**	1:30 - 3pm **PAPERS** **Scientific Applications II** • **Input/Output** • **Profiling**	10:30am - noon **PANEL** **Community Model Building**	
	1:30 - 3pm **PANEL**	1:30 - 3pm **PANEL**	3:30 - 5pm **PANEL**	10:30am - noon **PANELS**

	Experiences w/ Combining OpenMP and MPI	**Internet2 Status and Plans**	**It's the Software, Stupid: What We Really Need for Super Computing**	**Beyond Grids: Large-scale Computing in a Connected World** • **The IT Workforce - Where Have All the Geeks Gone?** • **Meet the CTOs**
	3:30 - 5pm **PAPERS** **Wide-area Applications** • **Numerical Algorithms I** • **MPI**	3:30 - 5pm **PAPERS** **High Perf. Networking** • **Scheduling II** • **Special Purpose Systems**	3:30 - 5pm **PAPERS** **Fernbach Award and Bell Finalists** • **Visualization** • **Commercial & Industrial Applications**	
	3:30 - 5pm **PANEL** **Telepathology and Medical Imaging for the Masses** • **digital.revolution.com: Transforming Science and Engineering**	3:30 - 5pm **PANEL** **Data Mining: The New Frontier for Supercomputing?**	Thursday, 6:30 - 10pm **SC99 RECEPTION** Open to all SC99 technical program registrants.	
Awards			1:30 - 3pm: **H. Fuchs** 3:30 - 5pm	
Poster, Research, Industry Exhibits	10am - 6pm	10am - 6pm 10 - 11am **Poster Reception**	10am - 4pm 10 - 11am **Poster Reception**	
Exhibitor Forum	10am - 5pm	10am - 5pm	10am - 4pm	
Registration & Store	7:30am - 6pm	7am - 6pm	7am - 5:30pm	8am - noon

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[tutorial abstract] Tuecke, Steve

[technical paper] Tufo, H. M.

[prize-winning paper] Tufo, H. M.

[student paper] Tullsen, Dean

[committee member] Turcotte, Louis

[technical paper] Turinsky, Andrei L.

[committee member] Zigler, Tami

[tutorial abstract] Zorn, Manfred

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MANAGING CREATIVITY

Donna Shirley
President, Managing Creativity

Donna Shirley, former manager of the Mars Exploration Program at the Jet Propulsion Laboratory and the original leader of the team that built the Sojourner Rover, will deliver the keynote address at SC99. Shirley retired from NASA last year and became a leading speaker and consultant on the management of creative enterprises. In addition to her autobiography, "Managing Martians," Shirley is the author of "Managing Creativity: A Practical Guide to Inventing, Developing, and Producing Innovative Products." Her talk will address how creative enterprises and their management must change as high-speed networks and computers become more pervasive.

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State of the Art of the Internet

Vinton G. Cerf, Senior Vice President, Internet Architecture and Technology for MCI WorldCom

The Internet can be understood from many perspectives. A brief historical view shows that it is still very immature in the commercial sense, despite its long technical history. Its current size and projected growth offer insights into how it may permeate our social and economic fabric as the next millennium unfolds. The technology of the Internet is adapting to support many modalities including voice/audio/radio, video, telephony, conventional web applications, real-time interaction (e.g. games, telepresence), email, and various kinds of transactions. The standards associated with the Internet are creating an information infrastructure in which new, value-added businesses can form. Virtual business organizations that draw upon network-enabled services are readily constructed. The Internet is even preparing to extend its reach off planet Earth, as well, as a part of the NASA Mars missions and more general exploration of the solar system. This talk will explore how the Internet is likely to evolve over the next four to six years and describe implications for how this evolution might affect scientific computing and other science industries that rely on the Internet.

- Bio: Vinton G. Cerf is the senior vice president of Internet Architecture and Technology for MCI WorldCom. Cerf's team of architects and engineers design advanced Internet frameworks for delivering a combination of data, information, voice, and video services for business and consumer use. Widely known as a "Father of the Internet," Cerf is the co-designer of the TCP/IP protocol, the computer language that gave birth to the Internet and which is commonly used today. In December 1997, President Clinton presented the U.S. National Medal of Technology to Cerf and his partner, Robert E. Kahn, for founding and developing the Internet.

  Prior to rejoining MCI in 1994, Cerf was vice president of the Corporation for National Research Initiatives (CNRI). As vice president of MCI Digital Information Services from 1982-1986, he led the engineering of MCI Mail, the first commercial email service to be connected to the Internet. During his tenure from 1976-1982 with the U.S. Department of Defense's Advanced Research Projects Agency (DARPA), Cerf played a key role leading the development of Internet and Internet-related data packet and security technologies. Cerf served as founding president of the Internet Society from 1992-1995 and is currently serving as the chair of its Board.

  Cerf is a member of the U.S. Presidential Information Technology Advisory Committee (PITAC) and the Advisory Committee for Telecommunications (ACT) in Ireland. He also sits on the Board of Directors for the Endowment for Excellence in Education, Gallaudet University, the MCI WorldCom

Foundation, and the Hynomics Corporation. Cerf is a fellow of the IEEE, ACM, and American Association for the Advancement of Science, the American Academy of Arts and Sciences and the National Academy of Engineering. Cerf holds a Bachelor of Science degree in mathematics from Stanford University and Master of Science and Ph.D. degrees in computer science from UCLA.

HPC meets .com: The Convergence of Supercomputing and Super-Internet Architectures

Greg Papadopoulos, Chief Technology Officer, Sun Microsystems

In this state-of-the-field talk, we will examine the watershed trend in high performance architecture: supercomputers created from internetworked high performance, yet commercial, computing platforms. The economics of hardware and software development argue that this approach will be with us for some time, so the evolution of high-end commercial computing platforms is of central importance to the future of HPC. What are the driving forces behind these platforms? How do we expect system architecture, interconnection networks, storage, and software stacks to evolve? This talk will focus upon answers for these questions.

A central thesis is that the requirements of HPC and large-scale Internet-based application service providers will mostly converge. Scales will be similar, and HPC users will enjoy the network and data centricity, and availability characteristics of Internet platforms. There is even speculation that new media datatypes will drive signal processing capabilities into commercial platforms that should be exploitable by HPC applications. The primary remaining issues will center on scaling for capability versus capacity, and the unique software requirements for HPC application development and runtime deployment.

- Bio: As chief technology officer, Greg Papadopoulos is responsible for assessing Sun's technological investments, as well as directing the activities of Sun Laboratories and associated advanced development programs. He also provides leadership and consistency for hardware and software architectures across Sun.

  Papadopoulos has held several positions at Sun since joining in 1994, including vice president of technology and advanced development for Sun's systems business; chief scientist for server systems engineering; and chief scientist for enterprise servers and storage. Before joining Sun, Papadopoulos was senior architect and director of product strategy for Thinking Machines. He was also an associate professor of electrical engineering and computer science at MIT, where he conducted research in scalable systems, multithreaded/dataflow processor architecture, functional and declarative languages, and fault-tolerant computing. He was a development engineer at Hewlett-Packard and Honeywell and co-founded three companies: PictureTel (video conferencing), Ergo (high-end PCs), and Exa Corporation (computational fluid dynamics).

  Papadopoulos holds a B.A. in systems science from the University of California, San Diego, and M.S. and Ph.D. degrees in electrical engineering and computer science from MIT.

Performance: Myth, Hype, and Reality

Daniel A. Reed, Professor and Head, Department of Computer Science, University of Illinois at Urbana-Champaign

"The most constant difficulty in contriving the engine has arisen from the desire to reduce the time in which the calculations were executed to the shortest which is possible." - Charles Babbage

Little has changed since Babbage's prescient remark. Performance optimization remains a difficult and elusive goal -- subtle interactions among parallel hardware and software components can easily lead to unexpected bottlenecks. Consequently, the history of parallel computing is replete with stories of application and system designs that failed to meet expected performance goals. Moreover, emerging applications are irregular, with complex, data-dependent execution behavior, and dynamic, with time varying resource demands. Concurrently, the scope of high performance computing is rapidly expanding from single parallel systems to distributed collections of heterogeneous sequential and parallel systems. This talk examines some of the reasons why obtaining high performance remains difficult, lessons from the history of high-performance computing, and the challenges for emerging systems. Throughout, we will highlight current approaches to understanding and improving performance. We will also suggest how things may change during the next five years.

- Bio: Dan Reed is currently professor and head of the Department of Computer Science at the University of Illinois at Urbana-Champaign. In addition, he holds a joint appointment as a senior research scientist with the National Center for Supercomputing Applications (NCSA) and is both a member of the executive committee and the leader of the distributed storage and distributed collaboration enabling technologies team for the National Computation Science Alliance, one of the two NSF PACI consortia. He is also a member of the steering committee for the DOE/ASCI ASAP Center for Simulation of Advanced Rockets (CSAR) at the University of Illinois.

  Reed is known for his contributions to the performance analysis of high performance parallel systems and his work on the analysis and optimization of parallel I/O systems. His work and that of others in the national Scalable I/O Initiative has led to the book, "*Scalable Input/Output: Achieving System Balance*." His Pablo project has developed portable performance data capture and presentation tools that have been one of the cornerstones of the national HPCC initiative. The resulting performance tools have been used to analyze virtual environments, optimize I/O performance, tune application performance, and study WWW server behavior. Current projects are exploring techniques for real-time closed loop and interactive adaptive control of applications and resource management policies for parallel systems. This work integrates dynamic performance instrumentation with real-time adaptive control mechanisms that select and configure resource management algorithms automatically, based on observed application behavior, or interactively, through virtual environments.

Distributed Data Mining: Problems And Opportunities

Salvatore J. Stolfo, Professor of Computer Science, Columbia University

Business, government, and science currently generate and make available online huge storehouses of data. Through Knowledge Discovery in Databases and Data Mining (KDD/DM) it has become possible to exploit automatic machine learning technologies to reveal novel patterns and nuggets of new information and knowledge of great scientific and commercial importance. Much progress has already been made in both the theory and practice of KDD/DM, including systems that can scale up machine learning to large corporate-sized data warehouses. Now attention has turned to the next level of complexity and scale: discovering new knowledge in very large and inherently distributed datasets. We will describe approaches to substantially increase the amount of data a knowledge discovery system can handle effectively over distributed data sources. However, numerous technical problems need to be solved for distributed data mining systems to be truly effective. In addition, the political and legal issues created by the advances in this field

must be understood and recognized for its potential dangers. Finally, we shall speculate about a new generation of KDD/DM systems that might begin to take shape in the next few years. We envision "data reactor" systems that will automatically generate new knowledge with little human intervention.

- Bio: Salvatore J. Stolfo is a professor of computer science at Columbia University where he has been on the faculty since 1979, immediately after receiving his Ph.D. from NYU's Courant Institute. He has published extensively in the area of parallel computing and AI. Stolfo co-developed the first Expert Database System in the early 1980s that was widely distributed to a large number of telephone wire centers around the nation. He also led a project that developed the 1023-processor DADO machine designed to accelerate knowledge-based and pattern-directed inference systems. DADO was one of the first massively parallel machines spawned by DARPA's Strategic Computing Program in the 1980s. His most recent research on distributed data mining has produced a system called JAM that has been widely deployed to research and development organizations. JAM has been applied to problems in fraud and intrusion detection in network information systems. His research has been supported by DARPA, NSF, ONR, NYSSTF, and a large number of industrial sponsors.

  Stolfo has advised more than a dozen Ph.D. students who hold academic, industrial research, and corporate positions. He has served as the chair of the Computer Science Department and as the Director of the Center for Advanced Technology at Columbia University. He was a member of the Citicorp Strategic Evaluation Program and an advisor to the Financial Services Technology Consortium. He is presently co-director of the USC/ISI and Columbia University Center for Applied Research in Digital Government Information systems, and PC co-chair of the SIGKDD 2000 conference. He has been awarded 10 patents in the areas of parallel computing and database inference and co-founded two high-tech companies.

Supercomputing on Windows NT Clusters: Experience and Future Directions

Andrew A. Chien, Science Applications International Corporation Chair Professor, University of California, San Diego

The rapid maturation of desktop and high-volume technologies in microprocessors, high-speed networks, and operating systems make commodity elements powerful building blocks for supercomputing systems. Windows NT clusters are attractive because of the wide range of commodity ISV software, widespread device support, and rich graphical environments. We will describe the design and experience of a very large NT cluster, built by CSAG and NCSA. Including the core cluster technologies (HPVM) and the system called the NT Supercluster:

- 256 Pentium family processors (~100 Gflops)
- 128 GB main memory, 1-4TB disk
- 2.4 Gbps switched network, 120 Gbps bisection bandwidth

We describe the evaluation of this system and its performance on a wide variety of scientific applications. Because there are many NT clustering efforts for high performance computing, we will also discuss a spectrum of commercial Windows NT cluster efforts and their experiences.

Footnote: The NT Supercluster was built in conjunction with the National Center for Supercomputing Applications (NCSA), demonstrated in April 1998, and has been available to users since December 1998. Rob Pennington leads the NT Supercluster effort at the Alliance Leading Edge Site (NCSA).

- Bio: Andrew A. Chien's research involves networks, network interfaces, and the interaction of communication and computation in high performance systems. Chien is the Science Applications International Corporation (SAIC) chair professor in the Department of Computer Science and Engineering at the University of California, San Diego. He received his undergraduate, master's, and doctoral degrees from the Massachusetts Institute of Technology in 1984, 1987, and 1990, respectively. From 1990 to 1998, Professor Chien was a faculty member in the Department of Computer Science at the University of Illinois and a senior research scientist in the National Center for Supercomputing Applications. He is currently working on large-scale clusters with both NCSA and NPACI. Andrew is also the recipient of a 1994 National Science Foundation Young Investigator Award, a 1995 C. W.

Gear Outstanding Faculty award, and a 1996 Xerox Outstanding Research Award.

100 Gbps or Bust: Building Wide Area High Performance Networks

Dona Crawford, Director, Advanced Product Realization Program, Sandia National Laboratories

Paper available

A strategy within the ASCI program calls for the use of very high performance computers at a distance. This requirement necessitates the creation of high performance wide area networks. This talk provides a background for the need to do distance computing, the technology roadmap to achieve the desired capabilities, and the planned methodology to reach 100Gbps by 2004.

- Bio: Dona Crawford is the director of the Advanced Product Realization Program and the Accelerated Strategic Computing Initiative (ASCI) Program at Sandia National Laboratories (SNL). SNL is a multiprogram national laboratory operated by Sandia Corporation, a Lockheed Martin Company for the U.S. Department of Energy. Crawford is responsible for focusing many of SNL's research and development activities, especially those relating to high performance computing and information technologies, in order to reduce the time and cost of the weapons life cycle, including design, assessment, manufacture, deployment and retirement. She started her career at Sandia in 1976 as a numerical analyst and has held several staff and management positions dealing with computing and information infrastructure, hardware servers, operating systems, visual comprehension, software environments, and engineering applications. More recently, Crawford was Sandia's representative on the ASCI Alliance Program at the beginning of the program, helping to establish a national university partnership to validate multidisciplinary simulation as a scientific methodology. She was also Sandia's lead to provide an environment to connect application developers and weapons designers to high-end computer resources running at teraflop speeds.

Merging Advanced Microscopy with Advanced Computing

Mark Ellisman, Professor of Neurosciences and Bioengineering; Director, Center for Research on Biological Structure; Director, National Center for Microscopy and Imaging Research, University of California, San Diego

Developments in modern computer-aided microscopies and advances in high performance computational infrastructure offer great promise for delivery of new information about the structural and functional dynamics of the nervous system. Neuroscientists are involved in research covering a wide range of scales, from modeling molecular events and subcellular organelles to mapping of brain systems. They are also interested in the ways in which single neurons and small networks of neurons process and store information. It is now possible to create detailed models of single neurons and to use these as the starting point for modeling the complex properties of neurons and neuronal networks. Breakthroughs in optical imaging methods and image processing have provided spectacular new opportunities for deriving information about the 3-D relationships between biological structures. Structure-function work is rapidly moving into the realm of 4-D imaging. Ellisman will describe the development of novel techniques for 3-D visualization of neuronal structures and modeling of their dynamic properties. He will place special emphasis on examples that involve the application of parallel processing and distributed computing.

- Bio: Mark H. Ellisman is a professor of neuroscience and bioengineering and the director of the Center for Research in Biological Structure at the University of California San Diego, where he has taught since 1977. He received his B.A. in 1970 in biological psychology from Berkeley and his Masters in neurophysiology in 1974 and Ph.D. in molecular, cellular and developmental biology in 1976 from the University of Colorado at Boulder, where he studied under Keith R. Porter. Ellisman now directs the National Center for Microscopy and Imaging Research (NCMIR), an internationally acclaimed technology development center and research resource established by the National Institute of Health (NIH). He has received numerous awards, including a Jacob Javits award from the NIH and the Creativity Award from the National Science Foundation; he is a Founding Fellow of the American Institute of Biomedical Engineering. He is the interdisciplinary coordinator for the National Partnership for Academic Computing Infrastructure (NPACI) and leads the Neuroscience thrust for the NPACI, which involves integration of brain research and advanced computing and communications technologies. His scientific contributions include work on basic molecular and cellular mechanisms of the nervous system and development of advanced technologies in microscopy and computational biology. He is a pioneer in the development of 3-D light and electron microscopy and combined application of these image acquisition tools and computational technologies to achieve greater understanding of the structure and function of the nervous system. His group was the first to introduce the idea of "telemicroscopy" by demonstrating the network-enabled remote use and sharing of a high-energy electron microscope in 1992 and then developing practical systems now in use by researchers in the US and abroad.

The ABC's of Large-scale Computing and Visualization: ASCI, Brains, Cardiology, and Combustion

Chris Johnson, Professor, Departments of Computer Science, Mathematics, Physics, and Bioengineering, University of Utah

The ASCI computers have speeds measured in teraflops and will handle dataset sizes measured in terabytes to petabytes. These machines offer enormous potential for solving very large-scale realistic modeling, simulation, and visualization. Similarly, since the inception of medical imaging, scanners have continually increased in their resolution capability. This increased image resolution has been instrumental in the use of 3-D images for diagnosis, surgical planning, and, with the advent of "open MRI systems," for surgery itself. The effectiveness of using such advanced hardware that produces large amounts of high-resolution data will hinge upon the ability of human experts to interact with their data and extract useful information. In this talk, Johnson will present new large-scale modeling, simulation, and visualization techniques for applications in computational combustion from the ASCI Center for the Simulation of Accidential Fires and Explosions (C-SAFE) and computational medicine from the Center for Scientific Computing and Imaging; he will also compare and contrast methods in computational combustion and medicine.

- Bio: Chris Johnson holds faculty appointments in the Departments of Computer Science, Mathematics, Physics, and Bioengineering at the University of Utah. His research interests are in the area of scientific computing, with particular interests in inverse and imaging problems, adaptive methods for partial differential equations, problem-solving environments, and scientific visualization. Johnson has received several awards, including: 1994 - NSF National Young Investigator (NYI) award; 1995 - NSF Presidential Faculty Fellow (PFF) award; 1996 - DOE Computational Science Award; 1997 - Par Excellence Award from the University of Utah Alumni Association and the Presidential Teaching Scholar Award; 1999 - Governor's Medal for Science and Technology, from the Governor of Utah. He directs the Center for Scientific Computing and Imaging at the University of Utah.

Human-competitive Machine Intelligence by Means of Parallel Genetic Programming

John R. Koza, Consulting Professor, Stanford Medical School; President, Third Millennium Venture Capital Limited

Genetic programming, operating on parallel computers, is now capable of automatically creating computer programs that are competitive with human-produced results in certain problem domains. This talk will introduce genetic programming; illustrate its application to problems of control, classification, system identification, and design; present some previously patented analog electrical circuits that have been automatically created using genetic programming; and describe the parallel computers (both transputer-based and beowulf-style) that have been used to produce these results.

- Bio: John R. Koza is currently a consulting professor of medical informatics at Stanford University where he teaches courses in genetic algorithms and computational molecular biology. He is the author of Genetic Programming: On the Programming of Computers by Means of Natural Selection (1992), Genetic Programming II: Automatic Discovery of Reusable Programs (1994), and co-author of Genetic Programming III: Darwinian Invention and Problem Solving (1999). Between 1973 and 1987, he was co-founder, chair, and chief executive officer of Scientific Games Inc. (NYSE company) and he is currently the president of Third Millennium Venture Capital Limited and a member of the Board of Trustees of the Santa Fe Institute.

Achieving Petaflops-scale Performance through a Synthesis of Advanced Device Technologies and Adaptive Latency Tolerant Architecture

Thomas Sterling, California Institute of Technology and NASA Jet Propulsion Laboratory

The achievement of Petaflops-scale computing is obstructed by the severe challenges of cost, size, power, complexity, reliability, efficiency, generality, and programmability. Even with the extraordinary rate of advance of CMOS technology and MPP architecture, practical systems capable of sustaining throughputs beyond a petaflops based on conventional technologies may not be feasible until sometime after 2010 and even then at a very high cost. An alternative strategy to exploit the superior properties of several advanced device technologies is under investigation by the HTMT interdisciplinary research project that has been sponsored by NSF, NASA, NSA, and DARPA. Such technologies include superconductor RSFQ logic, optical communications and holographic storage, and Processor-In-Memory SRAM and DRAM chips. Superconductor logic is capable of a hundred times the speed and power efficiency of conventional processors while fiber optical communications using time division and wave division multiplexing techniques can exceed wire-based channel bandwidth by a factor of a hundred or more. Optical storage density and power efficiency using holographic photorefractive techniques may provide an order of magnitude advantage over today's semiconductor memory at comparable bandwidths. But efficient computation requires effective resource management in the presence of extremes in latency and parallelism. The HTMT architecture has been devised to incorporate adaptive latency tolerant mechanisms based on the combination of multithreaded processors and an innovative memory-based proactive task management scheme called "Percolation." A detailed design study in combination with preliminary simulation and analysis indicates that practical petaflops-scale computing based on the HTMT model is feasible by 2005 with rapid advances leading beyond 10 petaflops likely shortly thereafter. This presentation will address the challenges imposed by the ambitious

goal of petaflops computing and discuss the opportunities afforded through alternative device technologies and the HTMT architecture strategy. Detailed findings from the HTMT project will be presented, demonstrating both the feasibility of implementation and practicality of use.

- Bio: Thomas Sterling received his Ph.D. from MIT in 1984 and has held research scientist positions with the Harris Corporation's Advanced Technology Department, the IDA Supercomputing Research Center, and the USRA Center of Excellence in Space Data and Information Sciences. In 1996 Sterling received a joint appointment at the NASA Jet Propulsion Laboratory's High Performance Computing group where he is a principal scientist and the California Institute of Technology's Center for Advanced Computing Research where he is a faculty associate. For the last 20 years, he has engaged in applied research in parallel processing hardware and software systems for high performance computing. Sterling was a developer of the Concert shared memory multiprocessor, the YARC static dataflow computer, and the Associative Template Dataflow computer concept and has conducted extensive studies of distributed shared memory cache coherence systems. In 1994, Sterling led the team at the NASA Goddard Space Flight Center that developed the first Beowulf-class PC clusters including the Ethernet networking software for the Linux operating system and is an author of the 1999 book, "How to Build a Beowulf" published by MIT Press. Since 1994, Sterling has been a leader in the national petaflops initiative chairing three workshops on petaflops systems development and chairing the subgroup on the petaflops computing implementation plan for the President's Information Technology Advisory Committee. He is also an author of the book, "Enabling Technologies for Petaflops Computing" published by MIT Press in 1995. Sterling is the principal investigator for the interdisciplinary Hybrid Technology Multithreaded (HTMT) architecture research project sponsored by NASA, NSA, NSF, and DARPA involving a collaboration of more than a dozen cooperating research institutions to develop a dynamic adaptive latency tolerant petaflops-scale computer employing superconductor, optical, and processor-in-memory technologies.

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  Rajive Bagrodia, Ewa Deelman, Thomas Phan - UCLA
  Rizos Sakellariou - Rice University

- **Locality Optimizations for Multi-Level Caches**
  Gabriel Rivera, Chau-Wen Tseng - University of Maryland

- **A Programmable Preprocessor for Parallelizing Fortran-90**
  Matt Rosing - PeakFive
  Steve B. Yabusaki - Pacific Northwest National Laboratory

GRID COMPUTING

- **A Network Performance Tool for Grid Environments**
  Craig A. Lee, James Stepanek - The Aerospace Corp.
  Rich Wolski - University of Tennessee
  Carl Kesselman - ISI/University of Southern California
  Ian Foster - Argonne National Laboratory

- **Multivariate Geographic Clustering in a Metacomputing Environment Using Globus**
  G Mahinthakumar, Forrest M Hoffman - Oak Ridge National Laboratory
  William W Hargrove - University of Tennessee
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- **Running EveryWare on the Computational Grid**
  Rich Wolski - University of Tennessee
  John Brevik - University of California, Berkeley
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  Marjory J. Johnson - RIACS/NASA Ames Research Center
  Matthew Chew Spence, Lawrence Chao - Raytheon/NASA Ames Research Center

- **H-RMC: A Hybrid Reliable Multicast Protocol for the Linux Kernel**
  Philip K. McKinley, Ravi T. Rao - Michigan State University
  Robin F. Wright - MIT

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  David Moran, Gary Ditlow, Daria Dooling, Ralph Williams, Tom Wilkins - IBM

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  Jose Moreira, Sam Midkiff, Manish Gupta, Rick Lawrence - IBM T. J. Watson Research Center

- **Industrial Seismic Imaging on Commodity Supercomputers**
  Scott A. Morton, Jeffrey R. Davis, Harry L. Duffey, Gary L. Donathan, Vic Forsyth, Steven N. Checkles - Amerada Hess Corporation

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  Tahsin Kurc, Chialin Chang, Renato Ferreira, Alan Sussman - University of Maryland
  Joel Saltz - University of Maryland, Johns Hopkins Medical Institutions

- **Informed Prefetching of Collective Input/Output Requests**
  Tara M. Madhyastha - University of California, Santa Cruz
  Garth A. Gibson, Christos Faloutsos - Carnegie Mellon University

- **Sun MPI I/O: Efficient I/O for Parallel Applications**
  Len Wisniewski, Brad Smisloff, Nils Nieuwejaar - Sun Microsystems Inc.

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- **MOM: a Matrix SIMD Instruction Set Architecture for Multimedia Applications**
  Jesus Corbal, Roger Espasa, Mateo Valero - Universitat Politecnica de Catalunya

- **A New Switch Chip for IBM RS/6000 SP Systems**
  Craig B. Stunkel - IBM T. J. Watson Research Center
  Jay Herring - IBM Server Group
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  Rajeev Sivaram - IBM Server Group

- **Scal-Tool: Pinpointing and Quantifying Scalability Bottlenecks in DSM Multiprocessors**
  Josep Torrellas, Yan Solihin, Vinh Lam - University of Illinois

MPI

- **MPI-2 implementation on Fujitsu generic message passing kernel**
  Noboru Asai - Fujitsu/SEL - Japan
  Thomas Kentemich - PALLAS - Germany
  Pierre Lagier - Fujitsu/FECIT - France

- **An Efficient Communication Architecture for Commodity Supercomputers**
  Stephan Brauss, Martin Lienhard, Josef Nemecek, Anton Gunzinger, Martin Näf - ETH Zurich
  Martin Frey, Martin Heimlicher, Andreas Huber, Patrick Müller, Roland Paul - Supercomputing Systems AG

- **BIP-SMP: High Performance Message Passing over a Cluster of Commodity SMPs**
  Patrick Geoffray, CNRS-INRIA ReMap project, RHDAC-University of LYON

Loïc Prylli, CNRS-INRIA ReMap project, UMR LIP - ENS LYON
Bernard Tourancheau, CNRS-INRIA ReMap project, RHDAC-University of LYON

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  Steve Sistare, Erica Dorenkamp, Nick Nevin, Eugene Loh - Sun Microsystems

- **Optimization of MPI Collectives on Clusters of Large-Scale SMP's**
  Steve Sistare, Rolf vande Vaart, Eugene Loh - Sun Microsystems, Inc.

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  Fatih Sevilgen - Syracuse Univeristy
  Srinivas Aluru - Iowa State University

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  Kang Su Gatlin, Larry Carter - University of California, San Diego

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  Zhao Zhang, Xiaodong Zhang - College of William and Mary

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  Mark Adams, Jim Demmel - University of California, Berkeley

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  George Biros, Omar Ghattas - Carnegie Mellon University

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  David Hysom, Alex Pothen - Old Dominion University, Norfolk VA

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  Ali Pinar, Michael T. Heath - Computer Science Dept. and Center of Simulation of Advanced Rockets, University of Illinois at Urbana-Champaign

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  Christian Weiss, Wolfgang Karl - LRR TUM, TU München
  Markus Kowarschik, Ulrich Rüde - Lehrstuhl fuer Systemsimulation, FAU Erlangen

- **Bounded-Error Compression of Particle Data from Hierarchical Approximate Methods**
  Dow-Yung Yang, Ananth Y. Grama- Computer Sciences Department, Purdue University
  Vivek Sarin - Texas A&M University

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  Chris H.Q. Ding, Yun He - Lawrence Berkeley National Laboratory
- **Performance Tuning and Evaluation of a Parallel Community Climate Model**
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  Patrick H. Worley - Oak Ridge National Laboratory
- **Simulated Circulation in the Indonesian Archipelago from a High Resolution Global Ocean General Circulation Model on the Numerical Wind Tunnel**
  Yukio Masumoto, Takashi Kagimoto, Toshio Yamagata - Frontier Research System for Global Change
  Masahiro Yoshida, Masahiro Fukuda, Naoki Hirose - National Aerospace Laboratory

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  Marcio Faerman, Alan Su - University of California San Diego
  Richard Wolski - University of Tennessee, Knoxville
  Francine Berman - University of California San Diego
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  Nicholas Mitchell, Larry Carter, Jeanne Ferrante, Dean Tullsen - University of California, San Diego
- **Performance Experiences on Sun's WildFire Prototype**
  Lisa Noordergraaf - Sun Microsystems - High End Server Engineering
  Ruud van der Pas - Sun Microsystems - European HPC Team
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  Leonid Oliker - NERSC-Lawrence Berkeley National Laboratory
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- **Parallel Sorting on Cache-coherent DSM Multiprocessors**
  Hongzhang Shan, Jaswinder P Singh - Princeton University
- **Architectural Requirements and Scalability of the NAS Parallel Benchmarks**
  Frederick C. Wong, Richard P. Martin, Remzi H. Arpaci-Dusseau, David E. Culler - University of

California, Berkeley

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  Karen Karavanic, Barton Miller - University of Wisconsin

- **Evaluating Titanium SPMD Programs on the Tera MTA**
  Carleton Miyamoto, Chang Lin - University of California, Berkeley

- **Managing Performance Analysis with Dynamic Statistical Projection Pursuit**
  Jeffrey Vetter, Daniel Reed - University of Illinois at Urbana-Champaign

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  Hubertus Franke, Joefon Jann, Jose Moreira, Pratap Pattnaik - IBM T. J. Watson Research Center
  Morris Jette - Lawrence Livermore National Laboratory

- **Scheduling Constrained Dynamic Applications on Clusters**
  Kathleen Knobe, James M. Rehg - CRL, Compaq Computer Corp.
  Arun Chauhan - Rice University
  Rishiyur S. Nikhil, CRL, - Compaq Computer Corp.
  Umakishore Ramachandran - Georgia Institute of Tech.

- **Job Scheduling in the Presence of Multiple Resource Requirements**
  William Leinberger, George Karypis, Vipin Kumar - Department of Computer Science and Engineering, University of Minnesota

- **Stochastic Scheduling**
  Jennifer M. Schopf - Northwestern University
  Francine Berman - UC San Diego

- **Adaptive Two-level Thread Management for Fast MPI Execution on Shared Memory Machines**
  Kai Shen, Hong Tang, Tao Yang - University of California, Santa Barbara

- **A Cost-Benefit Scheme for High Performance Predictive Prefetching**
  Vivekanand Vellanki - Georgia Institute of Techology
  Ann Chervenak - Information Sciences Institute, USC

SCIENTIFIC APPLICATIONS

- **Improved Parallel and Sequential Walking Tree Algorithms for Biological String Alignments**
  Paul Cull, Tai-Ching Hsu - Oregon State University

- **A Parallel Implementation of the TOUGH2 Software Package for Large Scale Multiphase Fluid and Heat Flow Simulations**
  Erik Elmroth, Chris Ding, Yu-Shu Wu, Karsten Pruess - Lawrence Berkeley National Laboratory

- **Direct Numerical Simulation of Turbulence with a PC/Linux Cluster: Fact or Fiction?**
  George-Sosei Karamanos, Constantinos Evangelinos, Richard C. Boes, Robert M. Kirby, George E. Karniadakis - Brown University

- **Scalable Electromagnetic Scattering Calculations on the SGI Origin 2000**
  John J. Ottusch, Mark A. Stalzer, John L. Visher, Stephen M. Wandzura - HRL Laboratories

- **An Object-Oriented Parallel Particle-in-Cell Code for Beam Dynamics Simulation in Linear Accelerators**
  Ji Qiang, Robert Ryne, Salman Habib - Los Alamos National Laboratory
  Viktor Decyk - University of California at Los Angeles

- **Large Scale Molecular Dynamics Simulations With Fast Multipole Implementations**
  Zhiqiang Wang, James Lupo, Alan McKenney, Ruth Pachter - AFRL/MLPJ

SPECIAL PURPOSE SYSTEMS

- **Mapping Irregular Applications to DIVA, A PIM-based Data-Intensive Architecture**
  Mary Hall, USC - Information Sciences Institute
  Peter Kogge, - University of Notre Dame
  Jeff Koller, Pedro Diniz, Jacqueline Chame, Jeff Draper, Jeff LaCoss, John Granacki - USC Information Sciences Institute
  Jay Brockman - University of Notre Dame
  Apoorv Srivastava, William Athas - USC Information Sciences Institute
  Vincent Freeh - University of Notre Dame
  Jaewook Shin, Joonseok Park - USC Information Sciences Institute

- **MOE: A Special-Purpose Parallel Computer for High-Speed, Large-Scale Molecular Orbital Calculation**
  Koji Hashimoto, Hiroto Tomita, Koji Inoue, Katsuhiko Metsugi, Kazuaki Murakami - Kyushu University
  Shinjiro Inabata, So Yamada, Nobuaki Miyakawa - Fuji Xerox Co.,Ltd
  Hajime Takashima, Kunihiro Kitamura - Taisho Pharmaceutical Co.,Ltd
  Shigeru Obara - Hokkaido University of Education
  Takashi Amisaki - Shimane University
  Kazutoshi Tanabe - NIMC
  Umpei Nagashima - National Institute for Advanced Interdisciplinary Research

- **A Personal Supercomputer for Climate Research**

James C. Hoe - MIT Lab for Computer Science
Chris Hill, Alistair Adcroft - MIT EAPS

VISUALIZATION

- **Adaptive, Multiresolution Visualization of Large Data Sets using a Distributed Memory Octree**
  Lori A Freitag, Raymond M. Loy - Argonne National Laboratory

- **Parallelization of Radiance For Real-Time Interactive Lighting Visualization Walkthroughs**
  David Robertson, Kevin Campbell, Stephen Lau, Terry Ligocki - Lawrence Berkeley National Laboratory

- **Numerical Simulation and Immersive Visualization of Hairpin Vortex Generation**
  H. M. Tufo - University of Chicago
  P. F. Fischer, M. E. Papka - Argonne National Laboratory
  K. Blom - Iowa State University

WIDE AREA APPLICATIONS

- **Papyrus: A System for Data Mining over Local and Wide Area Clusters and Super-Clusters**
  Stuart M. Bailey, Robert L. Grossman, Harinath Sivakumar, Andrei L. Turinsky - University of Illinois at Chicago

- **The Diesel Combustion Collaboratory: Combustion Researchers Collaborating over the Internet**
  Carmen M. Pancerella, Larry Rahn, Christine Yang - Sandia National Laboratories

- **DeepView: A Channel for Distributed Microscopy**
  B. Parvin, J. Taylor, G. Cong, M. O'Keefe and M. Barcellos-Hoff - Lawrence Berkeley National Laboratory

FERNBACH AWARD AND GORDON BELL FINALISTS

- **Multiscale Computational Cosmology with Adaptive Mesh Refinement (Fernbach Award)** - *paper not available*
  Michael Norman - University of Illinois at Urbana Champaign

- **$7.0/Mflops Astrophysical N-Body Simulation with Treecode on GRAPE-5**
  Atsushi Kawai, Toshiyuki Fukushige and Junichiro Makino - University of Tokyo

- **Terascale Spectral Element Algorithms and Implementation**
  H. M. Tufo - University of Chicago

P. F. Fischer - Argonne National Laboratory

- **Achieving High Sustained Performance in an Unstructured Mesh CFD Application**
  W. K. Anderson - NASA Langley Research Center
  W. D. Gropp - Argonne National Laboratory
  D. K. Kaushik - Argonne National Laboratory and Old Dominion University
  D. E. Keyes - Old Dominion University, Lawrence Livermore National Laboratory and NASA Langley Research Center
  B. F. Smith - Argonne National Laboratory

- **Very High Resolution Simulation of Compressible Turbulence on the IBM-SP System**
  A. A. Mirin, R. H. Cohen, B. C. Curtis, W. P. Dannevik, A. M. Dimits, M. A. Duchauneau, D. E. Eliason and D. R. Schikore - Lawrence Livermore National Laboratory
  S. E. Anderson, D. H. Porter and P. R. Woodward - University of Minnesota
  L. J. Shieh and S. W. White - IBM

Please report comments to sc99proceedings@sc99.org
Last Modified: Sep 27 1999

Tutorial Committee

Introduction from final program:

> This year's eight half-day and 12 full-day tutorials include outstanding offerings in new topics, such as file systems, computer and network security, NT and Linux Superclusters, and other computational grid applications, along with the return of the most requested presenters from prior years, with new and updated materials. Attendees also have the opportunity for an international perspective through tutorials on performance analysis tools and large data visualization. Separate registration is required for tutorials; tutorial notes and luncheons will be provided on site (additional tutorial notes will be sold on site). A One- or Two- day Tutorial Passport allows attendees the flexibility to attend several tutorials.

Tutorial abstracts are listed first by whether they were full day or half day tutorials and then in alphabetical order by first author's last name.

Full Day Tutorials

- High Performance Programming on SMPs - *M. Boucher, P. Hinker, J. Week*
- Concurrent Programming with Pthreads - *C. P. Breshears, H. A. Gabb*
- Introduction to Cryptography, Security, and Privacy Technologies - *C. E. Catlett*
- Running Applications on High-speed Networks--Theory, Practice, and Case Study - *J. Ferguson, M. Gates, J. Novotny, M. Thornton, M. Kutzo, T. Kazi*
- The Globus Grid Programming Toolkit - *S. M. Fitzgerald, C. Kesselman, I. Foster, G. von Laszewski, S. Tuecke*
- Introduction to High Performance Data Mining - *R. L. Grossman, V. Kumar*
- Parallel Computing Techniques to Maximize Your Megaflops - *C. Halloy, K. L. Wong*
- Framework Technologies and Large Data Visualization - *W.T. Hewitt, I. Curington*
- Parallel Programming with OpenMP - *T. Mattson, R. Menon, R. Eigenmann*
- Production Linux Clusters: Architecture and System Software for Manageability and Multi-user Access - *W. Saphir, P. Bozeman, R.Evard, P. Beckman*
- From Physics to File Systems - *R. Van Meter, P. Massiglia*
- Performance Analysis and Prediction for Large-scale Scientific Applications - *H. J. Wasserman, A. Hoisie*

Half Day Tutorials

- High Performance Computing with Legion - *A. Grimshaw*
- Tuning MPI Applications for Peak Performance - *W. Gropp, E. Lusk, R. Thakur*

- Real-world Scalable Parallel Computing - *A. E. Koniges, M. A. Heroux, W. J. Camp*
- High Performance Computing Facilities for the Next Millennium - *W. T. C. Kramer, J.Craw, K. Fitzgerald, F. Verdier*
- Performance Analysis and Tuning of Parallel Programs: Resources and Tools - *B. Mohr, B. Miller*
- Design and Analysis of NT and Linux Superclusters for Computational Grids - *R. L. Pennington, D. A. Bader, B. Maccabe*
- How to Run a Beowulf - *D. F. Savarese, T. L. Sterling*
- Computational Biology and High Performance Computing - *H. D. Simon, S. Spengler, M. Zorn, T. Head-Gordon, A. Arkin, B. Shoichet*

Full Day Tutorials

High Performance Programming on SMPs

Mike Boucher, Sun Microsystems
Paul Hinker, Sun Microsystems
Jeremy Week, Sun Microsystems

10% Introductory, 50% Intermediate, 40% Advanced

Abstract:

This tutorial will show participants how to get peak portable performance out of their cache-based microprocessor systems. Techniques to improve speed on both single-CPU systems (for MPI people) and SMP (for multithreaded people) will be covered. The focus will be on getting portable performance. This tutorial will give in-depth information on the operational characteristics of compilers, operating systems, hardware, and interconnects from the standpoint of an HPC programmer. The Compiler Essentials section will cover the structure of optimizing compilers. Participants will learn how compilers think about optimization and how to write code that can be optimized easily. Participants will see how subtle code changes can switch a code between structures that are easy or impossible to optimize. The Operating System Essentials section will described the things that an OS can do to help, what it can do to hurt, and how you can encourage one behavior or the other. The Hardware Essentials section will cover the features of systems based on microprocessors with caches and shows how to write code to take advantage of common hardware.

Concurrent Programming with Pthreads

Clay P. Breshears, Rice University/ERDC MSRC
Henry A. Gabb, Nichols Research Corporation/ERDC MSRC

65% Introductory, 35% Intermediate, 0% Advanced

Abstract:

Pthreads is a POSIX standard library for multithreading. Tasks are assigned to threads that execute concurrently. On symmetric multiprocessors, threaded tasks can execute in parallel. The Pthreads library consists of 61 functions governing thread creation and management, mutual exclusion, condition variables

and thread signaling, and low-level scheduling. The tutorial will cover design issues involved in concurrent and multithreaded programming, using Pthreads as a practical means of implementation. Before laying a foundation in concurrency, the tutorial will introduce fourteen core Pthreads functions most useful to scientific programming. Each function will be discussed in detail with example codes to illustrate usage. A detailed discussion of mutual exclusion variables will show how to avoid common race conditions like write/write and read/write conflicts. Lastly, condition variables and thread signaling will also be discussed. Classic concurrent programming models (e.g., producer/consumer) and problems (e.g., The Dining Philosophers) will illustrate the use of threads to express concurrent tasks. The pitfalls of race conditions and deadlock will be introduced and a series of examples will be presented to demonstrate the utility of Pthreads in scientific programming. Examples will include algorithms from the C3I Benchmark (terrain masking, route optimization, image correlation) as well as matrix multiplication and LU decomposition.

Introduction to Cryptography, Security and Privacy Technologies

Charles Catlett, National Computational Science Alliance

25% Introductory, 50% Intermediate, 25% Advanced

Abstract:

This tutorial provides an overview of the basic elements of computer security and privacy, including the building blocks, cryptographic technologies, and protocols used to construct secure and private services and systems. An overview of existing and emerging technologies and implementations of secure and private systems will be given. This will include both current practice and technologies (Java, Kerberos, PGP, SSL, etc.) and their application in the real world for secure computing as well as newer capabilities (digital cash, digital signatures) supporting commerce on the Internet. Participants should be familiar with networked computing (the Internet, client/server applications, etc.) as well as basic mathematics and computer programming. This basic background information is essential to anyone involved in the Internet today, including technical staff as well as executives.

Running Applications on High-Speed Networks - Theory, Practice, and Case Study

Jim Ferguson, National Laboratory for Applied Network Research
Mark Gates, National Center for Supercomputing Applications
Jason Novotny, National Center for Supercomputing Applications
Meghan Thornton, National Center for Supercomputing Applications
Mitch Kutzko, National Center for Supercomputing Applications
Tarique Kazi, National Center for Supercomputing Applications

15% Introductory, 45% Intermediate, 40% Advanced

Abstract:

This tutorial focuses on the most essential skills needed to develop applications for today's high-performance networks, such as vBNS and Abilene. The tutorial will give you a basic understanding of the TCP/IP protocol stack, high-speed networking, and common diagnostic tools. Included is a quick section on the BSD Socket programming interface in both C and Java using an effective learn-by-example strategy. An intermediate-level talk and hands-on lab follows, featuring tuning application performance for high-speed networks. Several case studies will be presented as examples of network applications, each in a different area. One case study covers real-time network performance monitoring tools (created by

NLANR) called Netlog and Viznet. Another case study will be Cactus, winner of an HPC Challenge Award at SC98. Cactus is an ambitious distributed astrophysical simulation which can run on multiple supercomputers. Other case studies will involve distributed immersive environments and a distributed remote process monitoring framework adapted by the DSRT scheduler that runs over the Globus infrastructure.

The Globus Grid Programming Toolkit

Steven Fitzgerald, University of Southern California - Information Sciences Institute
Ian Foster, Argonne National Laboratory
Gregor von Laszewski, Argonne National Laboratory
Carl Kessleman, University of Southern California - Information Sciences Institute
Steve Tuecke, Argonne National Laboratory

50% Introductory, 40% Intermediate, 10% Advanced

Abstract:

This tutorial is a practical introduction to programming for high-performance distributed computing systems, or "computational grids," and the capabilities of the Globus grid toolkit. Emerging high-performance networks promise to enable a wide range of emerging application concepts such as remote computing, distributed supercomputing, teleimmersion, smart instruments, and data mining. However, the development and use of such applications are, in practice very difficult and time consuming, because of the need to deal with complex and highly heterogeneous systems. The Globus grid programming toolkit is designed to help application developers and tool builders overcome these obstacles to the construction of "grid-enabled" scientific and engineering applications. It does so by providing a set of standard services for authentication, resource location, resource allocation, configuration, communication, file access, fault detection, and executable management. These services can be incorporated into applications and/or programming tools in a mix-and-match fashion to provide access to needed capabilities.

Introduction to High Performance Data Mining

Robert Grossman, University of Illinois at Chicago
Vipin Kumar, Univ. of Minnesota

50% Introductory, 30% Intermediate, 20% Advanced

Abstract:

Data mining is the semi-automatic discovery of patterns, associations, changes, anomalies, and statistically significant structures and events in data. Traditional data analysis is assumption driven in the sense that a hypothesis is formed and validated against the data. Data mining, in contrast, is discovery driven in the sense that patterns are automatically extracted from data. The goal of the tutorial is to provide researchers, practitioners, and advanced students with an introduction to data mining. The focus will be on algorithms, software tools, and system architectures appropriate for mining massive data sets using techniques from high performance computing. There will be several running illustrations of practical data mining, including examples from science, business, and computing. We will describe several architectural frameworks for high performance data mining systems and discuss their advantages and disadvantages. Finally, we will cover several case studies involving mining large data sets, from 10-500 Gigabytes in size.

Parallel Computing Techniques to Maximize Your Megaflops

Christian Halloy, JICS, University of Tennessee
Kwai L. Wong, University of Tennessee

50% Introductory, 30% Intermediate, 20% Advanced

Abstract:

Scientists can nowadays get fairly easy access to very powerful computing resources. However, the process of improving computer codes in order to maximize its megaflops rate is most often a challenging and complicated task. In this tutorial we will review general concepts of scientific computing and performance and introduce techniques that can significantly improve the performance. This tutorial will concentrate on three main topics:

- The math behind the program, or how simple changes in the numerical method can often improve speed and memory utilization.
- Improving single processor performance, by looking at issues such as memory management and data representations. Appropriate array indexing, loop unrolling, and other techniques will be analyzed and exemplified.
- Techniques that will improve parallel performance, looking into data parallel programming as well as message passing methodologies.

Problems due to data mapping and load balancing will also be reviewed. Many examples will be used to show the effects of different numerical methods and programming techniques on the performance of computer codes. We will conclude the tutorial by summarizing general strategies for obtaining improved performances.

Framework Technologies and Large Data Visualization

W. T. Hewitt, University of Manchester
I. Curington, AVS Inc

20% Introductory, 70% Intermediate, 10% Advanced

Abstract:

The presentation will address large data visualization issues in the context of commercial visualization tool development. A review of techniques for multidimensional data visualization will be followed by case studies from CEM, CFD, VLSI, Medicine, and Geophysics. An artifact of this type of visualization is that the visualization task itself becomes a consumer of HPC resources. The second part of the tutorial is concerned with the issues of implementing these techniques in a multiprocessor environment, and improving the performance of current visualization systems. A range of technical areas will be discussed, including experimental research and production algorithm development. Both current research and future challenges facing visualization system vendors will be discussed. Attendees at the tutorial will gain an understanding of the issues underlying visualization in a parallel and distributed environment including:

- Familiarity with domain decomposition methods and parallelization techniques
- Knowledge of the principles of volume, flow, and multidimensional visualization

- Ability to use distributed computation to enable accurate and timely visualization of large complex datasets
- Familiarity with the latest developments in visualization and HPC systems.

Parallel Programming with OpenMP

Tim Mattson, Intel
Ramesh Menon, Silicon Graphics, Inc
Rudolf Eigenmann, Purdue University

50% Introductory, 30% Intermediate, 20% Advanced

Abstract:

OpenMP is an Application Programming Interface for directive-driven parallel programming of shared memory computers. Fortran, C and C++ compilers supporting OpenMP are available for Unix and NT workstations. Most vendors of shared memory computers are committed to OpenMP making it the de facto standard for writing portable, shared memory, parallel programs. This tutorial will provide a comprehensive introduction to OpenMP. We will start with basic concepts to bring the novice up to speed and then move on to advanced topics. Over the course of the day, we will discuss:

- The OpenMP parallel programming model and its specification in Fortran, C and C++.
- Examples of OpenMP programs from scientific-engineering applications.
- The status of OpenMP compilers and tools.
- Future developments for OpenMP

Production Linux Clusters: Architecture and System Software for Manageability and Multi-User Access

William Saphir, Lawrence Berkeley Laboratory (NERSC)
Patrick Bozeman, Lawrence Berkeley National Laboratory (NERSC)
Remy Evard, Argonne National Laboratory
Pete Beckman, Los Alamos National Laboratory

30% Introductory, 50% Intermediate, 20% Advanced

Abstract:

Linux clusters have become a popular alternative to MPP and SMP servers for high-performance computing. Attracted initially by low hardware costs and the potential for high performance, many users find out later that clusters are a do-it-yourself affair. Information is scattered, and software is scattered and poorly integrated. The final result is often not robust or easily manageable. In this tutorial, we will guide you through the issues involved in setting up and running a cluster. The emphasis will be on understanding choices and tradeoffs in manageability, functionality, and performance, and on the interaction and integration of various components. We will present an overview of cluster architectures, system software, and application-level software. Our goal is not to be comprehensive, covering every half-baked piece of

experimental cluster software, but to describe software and architectures that work, allowing you to focus on high performance computing rather than system administration. The first half-day of the tutorial will be a lecture/discussion. The second half-day will be a workshop in which we will guide participants through a hands-on cluster installation and configuration.

From Physics to File Systems

Rodney Van Meter, Quantum Corp.
Paul Massiglia, Quantum Corporation

20% Introductory, 50% Intermediate, 30% Advanced

Abstract:

"From Physics to File Systems" provides an overview of storage and I/O systems, starting with the physical building blocks of buses, networks, disks and tapes and ending with hierarchical storage management systems and distributed file systems. The presentation will be organized around the three themes of data movement, data storage, and data management. In data movement, attendees will learn about buses, networks, device drivers and other elements required to move data from applications to non-volatile storage. The data storage segment will cover physical storage technologies, such as magnetic disks and tapes, auto-changers, and the structure of RAID subsystems. After providing the description of the technologies for storing a moving data, the data management segment will describe how these become complete systems. Local file systems will be investigated in detail, both their on-disk formats and kernel implementations, then distributed file systems and finally hierarchical storage management systems. Throughout this segment, examples will be drawn from many varieties of Unix systems and Windows NT, with occasional notes from the VMS and supercomputing worlds.

Performance Analysis and Prediciton for Large Scale Scientific Applications

Harvey J. Wasserman, Los Alamos National Laboratory
Adolfy Hoisie, Los Alamos National Laboratory

30% Introductory, 50% Intermediate, 20% Advanced

Abstract:

We will present a methodical, simplified, approach to analysis and modeling of large-scale, parallel, scientific applications. Various techniques (modeling, simulation, queuing theory), will be discussed so as to become a part of the application developer's toolkit. We will introduce rigorous metrics for serial and parallel performance and analyze the single most important single-processor bottleneck - the memory subsystem. We will demonstrate how to obtain diagnostic information about memory performance of codes and how to use such information to bound achievable performance. Commonly-utilized techniques for performance optimization of serial and parallel Fortran codes will also be presented. Finally, we will discuss analytical modeling of application scalability using ASCI codes as examples. No particular machine will be emphasized; rather we will consider RISC processors and widely utilized parallel systems, including clusters of SGI Origin2000s, IBM SP2 and CRAY T3E.

High Performance Computing with Legion

Andrew Grimshaw, University of Virginia

90% Introductory, 10% Intermediate, 0% Advanced

Abstract:

Legion is an integrated metasystem or "grid" system that has been deployed at a number of sites. Legion supports existing codes written in MPI and PVM, as well as legacy binaries. Key capabilities include: Legion eliminates the need to move and install binaries manually on multiple platforms; Legion provides a shared, secure virtual file system that spans all the machines in a Legion system; Legion provides strong PKI-based authentication and flexible access control for user objects; and Legion supports remote execution of legacy codes, and their use in parameter space studies. A variety of diverse applications have been ported to Legion, e.g., CHARMM, ocean models, CCM, particle-in-cell codes, and several parameter space studies. This tutorial will provide background on the Legion system and teach how to run existing parallel codes within the Legion environment. The target audience is supercomputer users who are already familiar with parallel processing tools such as MPI and PVM. The tutorial will consist of an introduction to the Legion system, philosophy, architecture, and the object model.

Tuning MPI Applications for Peak Performance

William Gropp, Argonne National Laboratory
Ewing Lusk, Argonne National Laboratory
Rajeev Thakur, Argonne National Laboratory

0% Introductory, 50% Intermediate, 50% Advanced

Abstract:

Both applications and important benchmarks are being ported from other message-passing libraries to MPI. In most cases it is possible to make a translation in a fairly straightforward way, preserving the semantics of the original program. On the other hand, MPI provides many opportunities for increasing the performance of parallel applications by the use of some of its more advanced features. An understanding of performance-critical issues for message-passing programs, both for communication and I/O, can provide the application programmer with the ability to provide a greater percentage of the peak performance of the hardware to the application while still relying on MPI to provide portability. This tutorial will discuss performance-critical issues in message passing programs, explain how to examine the performance of an application using MPI-oriented tools, and show how the features of MPI can be used to attain peak application performance. We will assume knowledge of MPI, particularly MPI-1. We will explain how to take advantage of various options in MPI. In the MPI-2 area, we will focus on parallel I/O, where implementations are now widely available.

Real World Scalable Parallel Computing

Alice E. Koniges, Lawrence Livermore National Laboratory
Michael A. Heroux, Sandia National Laboratories
William J. Camp, Sandia National Laboratories

25% Introductory, 50% Intermediate, 25% Advanced

Abstract:

In the introductory material, we will provide an overview of the terminology, hardware, performance issues, programming models, and software tools available for large-scale application computing. We will include comparisons of the various ASCI platforms and industrial set-ups in both Europe and the US. Next, we will draw from a series of 25 large-scale applications codes and discuss specific challenges and problems encountered in parallelizing these applications. The application areas will be a mix of industrial and government applications including aerospace, biomedical sciences, materials processing and design, plasma and fluid dynamics. We will discuss how to determine the best choice of programming model (e.g. MPI, OPEN-MP, Threads) for a given application while maintaining portability. Specific details of coding comparisons in the various models will also be provided. We will detail real experiences in debugging/tuning large-scale applications and what to expect in actual performance and will discuss choices for large-scale codes in terms of interpretative languages and parallel I/O libraries. Finally, we will end with a summary of the lessons learned from these applications and predictions for the future of high-performance computing.

High Performance Computing Facilities for the Next Millenium

William Kramer, Lawrence Berkeley National Laboratory
James Craw, Lawrence Berkeley National Laboratory
Keith Fitzgerald, Lawrence Berkeley National Laboratory
Francesca Verdier, Lawrence Berkeley National Laboratory

0% Introductory, 100% Intermediate, 0% Advanced

Abstract:

HPC facilities face increased pressures so must combine effective techniques of the past with innovative methods of the future to survive and thrive in the next millennium. This tutorial will explore requirements and pressures on HPC centers, present effective methods being employed and new approaches to employ to overcome these challenges.

Topics will include:

- The current state of HPC computing and projections.
- System management methods that make it possible to achieve CPU utilization greater than 90% for MPPs running many large jobs.
- Archive storage issues for improving transfer bandwidth and practical advice for running Terabyte archives.
- Innovations in client services to ensure the "intellectual resource" is valued equally with Gigaflop/s and Terabytes by the users of the system.
- Introductions to the Effective System Performance test, a new way to objectively measure and compare not just system performance (e.g. sustained performance of applications) but also system effectiveness (e.g. how many system resources, especially CPU time, can be used by the workload)

- How to achieve and maintain the delicate balance needed to integrate production facilities with a good research and development program

It will also explore what a HPC facility needs to do to thrive in the new millennium.

Performance Analysis and Tuning of Parallel Programs: Resources and Tools

Bernd Mohr, Research Centre Juelich
Barton Miller, University of Wisconsin-Madison

50% Introductory, 30% Intermediate, 20% Advanced

Abstract:

This tutorial will give a comprehensive introduction into the theory and practical application of the performance analysis, optimization, and tuning of parallel programs on currently used high-end computer systems like the IBM SP, SGI Origin, and CRAY T3E as well as clusters of workstations. We will introduce the basic terminology, methodology, and techniques of performance analysis and give practical advice on how to use these in an effective manner. Next we will describe vendor, 3rd party, and research tools available for these machines along with practical tips and hints for their usage. We will show how these tools can be used to diagnose and locate typical performance bottlenecks in real-world parallel programs. Finally, we will give an overview of Paradyn, an example of a next generation performance analysis tools that can be used for parallel programs of today. The presentation will also include the Performance Consultant that automatically locates the performance bottlenecks of user codes.

Design and Analysis of NT and Linux Superclusters for Computational Grids

Robert L. Pennington, National Center for Supercomputing Applications
David A. Bader, The University of New Mexico
Barney Maccabe, The University of New Mexico

10% Introductory, 50% Intermediate, 40% Advanced

Abstract:

The Alliance has constructed two superclusters to run MPI-based scientific problems for the National Computational Grid. The goal of both clusters is to provide easy-to-use high performance computing systems at reasonable prices. Superclusters are large-scale clusters built with commodity PCs and high performance interconnects. The NCSA and UNM Superclusters use Intel processors and Myricom's Myrinet interconnect. The NCSA Supercluster is based on Windows NT and uses commercial off-the-shelf deskside systems from HP. The software includes job scheduling with LSF from Platform Computing, and an MPI implementation based on the High Performance Virtual Machine (HPVM) from Andrew Chien's CSAG research group. The University of New Mexico Supercluster is based on Linux and was integrated by Alta Technology. Portable Batch System (PBS) schedules the machine using a Maui Scheduler plug-in module and has an implementation of MPICH on top of Myrinet GM drivers. We will discuss the details on the construction, configuration and management of these systems. Details on porting applications to the superclusters will be provided.

How to Run a Beowulf

Daniel Savarese, Caltech
Thomas L. Sterling, Caltech

30% Introductory, 40% Intermediate, 30% Advanced

Abstract:

The construction of commodity clustered computing systems in lieu of the purchase of prefabricated supercomputers has grown in popularity in recent years among both research institutions and industry. Clusters delivering 10 Gflops peak can be assembled for a total cost under $30,000. However, the total cost of ownership of such systems can vary greatly depending on system maintenance procedures and Supporting software. In addition, while the hardware assembly of clusters has become relatively standard, the complete system architecture, including system and applications software installation and configuration, can differ significantly among clusters. Even though many clusters are used primarily as supercomputer replacements intended to run computational simulations, other uses are becoming more common, dictating different software organization schemes and maintenance procedures. In this half-day tutorial, we will describe how to keep a Beowulf cluster running, focusing on system software configuration and administration strategies aimed at reducing total cost of ownership. An emphasis will be placed on clusters used for running computational simulations, but some time will be dedicated to discuss alternate configurations.

Computational Biology and High Performance Computing

Horst D. Simon, Lawrence Berkeley National Laboratory (NERSC)
Sylvia Spengler, Lawrence Berkeley National Laboratory (NERSC)
Manfred Zorn, Lawrence Berkeley National Laboratory (NERSC)
Teresa Head-Gordon, Lawrence Berkeley National Laboratory (NERSC)
Adam Arkin, Lawrence Berkeley National Laboratory (NERSC)
Brian Shoichet, Northwestern University

30% Introductory, 40% Intermediate, 30% Advanced

Abstract:

The pace of extraordinary advances in molecular biology has accelerated in the past decade due in large part to discoveries coming from genome projects on human and model organisms. The advances in the genome project so far, happening well ahead of schedule and under budget, have exceeded any dreams by its protagonists, let alone formal expectations. Biologists expect the next phase of the genome project to be even more startling in terms of dramatic breakthroughs in our understanding of human biology, the biology of health and of disease. Only today can biologists begin to envision the necessary experimental, computational and theoretical steps necessary to exploit genome sequence information for its medical impact, its contribution to biotechnology and economic competitiveness, and its ultimate contribution to environmental quality. High performance computing has become one of the critical enabling technologies, which will help to translate this vision of future advances in biology into reality. Biologists are increasingly becoming aware of the potential of high performance computing. The goal of this tutorial is to introduce the exciting new developments in computational biology and genomics to the high performance computing community.

Last Modified: Oct 16 1999

The SC99 Awards Session will include awards for national contributions to HPC, as well as the results of conference competitions.

Seymour Cray Computer Engineering Award

> SC99 will present the ***first*** annual IEEE Computer Society Seymour Cray Computer Engineering Award. This award is presented in recognition of innovative contributions to high performance computing systems that best exemplify the creative spirit demonstrated by Seymour Cray. This award, which consists of a crystal memento, illuminated certificate, and $10,000 honorarium, is funded from an endowment provided by Silicon Graphics Inc. Additional information and nomination instructions are available at http://computer.org.

Sid Fernbach Award

> SC99 will also host the annual IEEE Computer Society Sid Fernbach award. This honors Sidney Fernbach, one of the pioneers in the development and application of high performance computers for the solution of large computational problems. It is given annually to someone who has made "an outstanding contribution in the application of high performance computers using innovative approaches."

This year's winner is Prof. Michael Norman of the University of Illinois at Urbana Champaign, whose paper *Multiscale Computational Cosmology with Adaptive Mesh Refinement* was presented at the conference.

Gordon Bell Prize

> The Gordon Bell Prize was instituted in 1988 by Dr. Gordon H. Bell, one of the designers of the DEC Vax computer systems, and along-time patron of the field of high performance computing. He offered $1000 of his own funds annually to recognize top achievements in high performance scientific computing. Technical Paper entries to the Bell prize are judged annually by a panel of three respected figures in high performance computing. While the principal prize is for total sustained performance, prizes have also been awarded in such categories as compiler speedup. For the 1999 Gordon Bell Prize, Dr. Bell has increased the stipend to $5000. For information about next year's (SC2000) Gordon Bell Prize, please contact Jim McGraw at jmcgraw@llnl.gov.

The finalists for this year's prize are

- **$7.0/Mflops Astrophysical N-Body Simulation with Treecode on GRAPE-5**
  Atsushi Kawai, Toshiyuki Fukushige and Junichiro Makino - University of Tokyo
- **Terascale Spectral Element Algorithms and Implementation**
  H. M. Tufo - University of Chicago
  P. F. Fischer - Argonne National Laboratory
-

Achieving High Sustained Performance in an Unstructured Mesh CFD Application
W. K. Anderson - NASA Langley Research Center
W. D. Gropp - Argonne National Laboratory
D. K. Kaushik - Argonne National Laboratory and Old Dominion University
D. E. Keyes - Old Dominion University, Lawrence Livermore National Laboratory and NASA Langley Research Center
B. F. Smith - Argonne National Laboratory

- **Very High Resolution Simulation of Compressible Turbulence on the IBM-SP System**
A. A. Mirin, R. H. Cohen, B. C. Curtis, W. P. Dannevik, A. M. Dimits, M. A. Duchauneau, D. E. Eliason and D. R. Schikore - Lawrence Livermore National Laboratory
S. E. Anderson, D. H. Porter and P. R. Woodward - University of Minnesota
L. J. Shieh and S. W. White - IBM

Best Paper Awards

$1,000 will be awarded for the paper selected by the technical papers committee as "best paper of conference."

A second award, for the best paper with a student as principal author, will be made, and includes all of the following:

- $500
- membership in the next year's Tech Papers Committee
- a paid trip to the Committee meeting to review papers
- a paid trip to the next year's conference

HPC Games Awards

In addition, several awards will be made in conjunction with the conference's HPC Games challenge. All winners will be announced at the SC99 Awards Session.

For more information....

Nominations for the Seymour Cray award
Nominations for the Sid Fernbach award
HPC Games opportunities

Please report comments to sc99proceedings@sc99.org
Last Modified: Thu Aug 12 1999

Panels let SC99 attendees become more involved in the conference by providing opportunities to hear from HPNC leaders and to interact with them via question-and-answer sessions.

Beyond Grids: Large-scale Computing in a Connected World

Grids offer a scale of computing not considered before that raises a host of serious issues, including resource management and programmability, not to mention application performance and scalability in an environment with a deep latency hierarchy. These issues, however, are not unique to grid environments. Large-scale supercomputing faces many of the same problems in terms of a deepening memory hierarchy and getting the right data to the right processors fast enough as dictated by the application's data locality and the available bandwidth and latency. While it will certainly be possible to implement applications in these environments, what are the wider abstractions that will allow programming models and run-time systems to best utilize standard performance techniques, e.g., multithreading, caching, and prefetching, and how should systems be designed and built to better support those abstractions?

Discussion questions include:

- What processor architecture (and device technologies) will be needed to handle bandwidths and latencies not only in petaflop systems but also in grid environments?
- How should primary and secondary storage be organized and accessed in petaflop and Grid computing environments?
- How should network protocols (and OSs) change to support Grid computations better?
- Is message-passing it? Can other programming models be effectively supported in a petaflop/Grid computing environment with a deep memory hierarchy? How can latency tolerance be integrated into the programming model?
- Will applications be able to effectively manage their resources and generate enough concurrency to

utilize a petaflop grid?
- Should there be a clear "division of labor" among network protocols, runtime systems, middleware, and applications, or should there be some integration of functionality for performance?
- Will mainstream "commodity" computing, both software and hardware, move in this direction or will the economic realities of the mass market dictate the shape of large-scale Grid computing?

MODERATOR
Craig Lee, Aerospace Corp.
PANELISTS
Reagan Moore, NPACI/SDSC
Carl Kesselman, USC/ISI
Dan Reed, U. Illinois at Urbana-Champaign
Chuck Seitz, Myricom, Inc.
Thomas Sterling, Caltech and JPL

Bioinformatics and High Performance Computing

The panel will discuss big computations in the biological sciences. Examples include: sequence analysis-searching of large sequence databases, classification of sequences into families, assembly of sequence fragments, annotation of genomes; and protein structure-folding, threading, and search pattern discovery in gene expression data genetic mapping using very large numbers of markers in very large populations. We will also attempt to identify grand challenge problems that could excite the scientific community and be a vehicle to increase interest in the area.

MODERATOR
Nathan Goodman, Compaq Computer Corp.
PANELISTS
Alan Heirich, Compaq Tandem Laboratories
Robert Kuhn, Kuck & Associates, Inc.
George Michaels, Monsanto
Gary Montry, Southwest Parallel Software
Andrew H. Sherman, Scientific Computing Associates, Inc.

Challenges and Opportunities of the Scalable Information Infrastructure

The President's Information Technology Advisory Committee (PITAC) report identifies the emerging Scalable Information Infrastructure (SII) as a critical component element. The SII is predicated on more than just the development of a faster Internet-it also requires advances in basic networking technology; scaling of network infrastructure in all dimensions, including size, speed, heterogeneity, and services; increased reliability and security; the development of middleware and services to support large-scale systems; and the development of large-scale applications.

In this panel, we explore the SII vision as suggested by the PITAC report, discussing the major obstacles that must be overcome to develop, construct, deploy, and apply a future SII. We discuss the potential shape of the SII (Web on steroids, or some new type of infrastructure such as the Grid), the models that may be followed to construct and finance it, and the new opportunities that it may expose for progress in both science and industry.

MODERATOR
Ian Foster, ANL and U. Chicago
PANELISTS
Ken Kennedy, Rice U. and PITAC
Carl Kesselman, USC/ISI

Dave Farber, U. Pennsylvania

Community Model Building

Computer modeling and simulation has traditionally been a tool used by individual and small groups of scientists to advance their research. In recent years, it has become more common to see teams of scientists in a particular discipline attempt to build community-wide models and information resources that encapsulate not just the work of one group, but represent the state-of-the-art level of understand of the community as a whole. A prototype and touchstone of this development is the GCM-the Global Circulation Model, which has been successful in the area of weather and climate modeling.

This panel brings representatives from two fields-earthquake modeling and space weather modeling-which are beginning to make this transition together with the computational scientists and infrastructure builders who are enabling it. Some key questions to be discussed by the panel are:

- What makes a scientific field "ready" for the transition to a community model?
- What are the steps a community must take to build and maintain such a model?
- What are the key improvements in computation that would enhance the transition in your field?

MODERATOR
Roscoe Giles, Boston U.
PANELISTS
John Rundle, U. Colorado
Chuck Goodrich, U. Maryland
Geoffrey Fox, Syracuse U./NPAC

Data Mining: The New Frontier for Supercomputing?

Explosive growth in the availability of online data has provided an unprecedented opportunity to mine this data to extract more intelligent and useful information. Due to the huge size of data and amount of computation involved, high performance computing is an essential component for many large-scale data mining applications. In fact, such applications are poised to become the dominant consumers of supercomputing in the near future. In contrast, the market for traditional scientific applications that have driven the field of supercomputing for the past several decades has been relatively static. Furthermore, data mining offers great possibilities for detecting useful patterns from the mass of data produced by scientific simulations conducted on high performance computers.

The panel will bring together experts from national and DoD labs, industry, and academia to discuss the role of data mining and its potential impact on the field of supercomputing. Specifically, the panel will address the following questions: What data mining applications have the potential of becoming the dominant consumers of supercomputing cycles over the next decade? What demands do these applications place on the architectures and environments of parallel computing? Are the desired features of parallel architectures and environments for data mining fundamentally different than those used for traditional scientific computing applications? To what extent can data mining help in analyzing the mass of data produced by scientific simulations?

MODERATOR
Vipin Kumar, Army High Performance Computing Research Center and U. Minnesota
PANELISTS
Alok Choudhary, Northwestern U.
Jaiwei Han, Simon Fraser U.
Robert Hollebeek, U. Pennsylvania

Raju Naburu, Army Research Lab

digital.revolution.com: Transforming Science and Engineering

In February 1999 the President's Information Technology Advisory Committee (PITAC) released its report, "Information Technology Research: Investing in Our Future." This report, which has been widely circulated and frequently quoted, has been instrumental in designing both the President's proposed Information Technology for the 21st Century (IT-squared) initiative and the proposed Congressional Networking and Information Technology Research and Development Act. In this panel, PITAC members will discuss their report, Congressional reaction to it, and their plans. The committee will answer questions provided in advance, followed by an open mike session for questions from the floor. The report and further information about the PITAC, including a link to the draft legislation and its status report, can be found at: http://www.ccic.gov/ac/

MODERATOR
Steve Wallach, Centerpoint, Inc.
PANELISTS
David Cooper, LLNL
Susan Graham, UC Berkeley
Ken Kennedy, Rice U.
Larry Smarr, NCSA
Joe Thompson, Mississippi State U.

Experiences with Combining OpenMP and MPI

To use the full capabilities of new high-end systems from Beowulf clusters to ASCI systems, it is important to use two levels of parallelism: distributed memory with message passing (e.g. MPI), and shared memory with threading (e.g. OpenMP). We have collected several applications that demonstrate various approaches to using hybrid parallelism. This panel will discuss lessons learned in developing and running some of these applications. Fundamental questions to be addressed include:

- How does the application use hybrid parallelism? Discuss in principle and in practice, showing example(s).
- What are the tradeoffs in using each model? Discuss strengths and weaknesses of each level. When is it better to use both?
- What performance scalability have you obtained? How much work has it taken?
- What limitations do you see to using hybrid parallelism? What is needed for the future?

Panelists experienced with combining DMP and SMP models will address a range of approaches to developing parallelism. Panelists include the developer/user, the professional developer, the performance analyst, and the end user.

MODERATOR
Robert H. Kuhn, Kuck & Associates, Inc.
PANELISTS
Henry Gabb, Corps of Engineering, Waterways Experiment Station
Greg Gaertner, Compaq Computer Corp.
John Levesque, IBM
Ramesh Menon, SGI
Stef Salvini, Numerical Algorithms Group, Inc.
Howard Scott, LLNL

Internet2 Status and Plans

Internet2 staff members will provide updates on:

- Internet2 status (number of members, new initiatives).
- Applications and engineering working groups (highlights of activities in digital video, distributed storage, quality of service and the Qbone initiative, routing).
- Update on Abilene (speeds, connection points, number of connections).
- Federal relations (status of peering agreements, connections at Next Generation Internet exchanges, outcomes from the August applications workshop).
- International relations (status of international peering, the various connection points in the U.S., including the STARTAP in Chicago and the Hudson St. facility in New York City).

MODERATOR
Ted Hanss, Internet2
PANELISTS
Guy Almes, Internet2
Paul Love, Internet2
Ben Teitelbaum, Internet2

It's the Software, Stupid: What We Really Need for Super Computing

As noted by the President's Information Technology Advisory Committee, software is the key bottleneck in effectively using computers. Current programs are too slow, too unreliable, too hard to use, and too limited. As high performance computing moves to a more networked, more complex, world and more ambitious, more complicated applications, the bottlenecks threaten to get worse. Fortunately, we can count on software researchers to attack and defeat these problems, just as they attacked and defeated the Y2K bug. Uh, wait a minute... This panel will describe what makes software so hard for distributed computing, programming tools, user interfaces, and other areas. The Panelists will then venture their best guesses about how we can make software easier.

MODERATOR
Chuck Koelbel, NSF
PANELISTS
Eric Brewer, Inktomi
Fran Berman, UCSD
Sven Hammarling, NAG Software
Dan Reed, U. Illinois at Urbana-Champaign
Andy Van Dam, Brown U.

Meet the CTOs

Listen to and interact with CTOs (Chief Technology Officers) as they discuss the following issues:

CTO Responsibility

- Direct the technical vision and direction of a company in hardware, software, and systems
- Be aware of market trends
- Help establish industry standards
- Promote their company's technology

Issues in High Performance Systems

- RISC vs. vector
- Commodity vs. proprietary processors

- Interconnection architectures
- SMPs, clusters, or a combination
- Unix (Linux) vs. WNT (VMS+)
- Applicability for both commercial and technical application
- TOPS 500
- TPC - C/D

2010

- PetaFlops computing?
- The Grid takes over?
- Major paradigm shifts in technology and new killer applications
- Next Generation Internet (NGI)
- 3-D images
- Virtual workplace
- Tele-immersion

MODERATOR
Steve Wallach, Centerpoint, Inc.
PANELISTS
Yoshiro Aihara, Hitachi
Greg Astfalk, Hewlett-Packard
Bill Blake, Compaq Computer Corp.
John Mashey, SGI
Jamshed Mirza, IBM Corp.
Kenichi Miura, Fujitsu Limited
Burton Smith, Tera Computer Corp.
Tadashi Watanabe, NEC Corp.

Telepathology and Medical Imaging for the Masses

This panel will examine several telepathology applications demanding large data stores, high bandwidth transport, and often high performance computers. More and more, medical practice, whether civilian or military, will require routine access to special expertise that will only be affordable when high performance networks are used to access centers of excellence. Examples of demands will include emergency response to bio-terrorism, centralized forensic pathology expertise, and access to extensive histological samples for education, diagnostic support, and surgical planning. As one example, the Visible Embryo project is exploring the needs of telepathology. The project goal is to digitize 100 years of human developmental pathology specimens and reconstruct 3-D models of the embryos to support embryology research education and training. Each digitized embryo requires up to 8 terabytes of storage when digitized at histological resolution. Experts are examining the digitized images, often requesting online access to the digitizing microscope to select improved focal planes to capture the features of specific developing organ systems. The panel will present specific examples from the Visible Embryo project, tools and experience with the Visible Human project, the needs of a tele-forensics-pathology program, and the role of the NTON and its peer networks in realizing the projects' objectives. Live access over the NTON will be demonstrated.

MODERATOR
George Michaels, George Mason University
PANELISTS
Bill Oliver, Armed Forces Inst. of Pathology
Michael Doyle, EOLAS Technologies
David Thornburg, Oregon Health Sciences U.

Bill Lennon, LLNL

The IT Workforce - Where Have All the Geeks Gone?

The recent President's Information Technology Advisory Committee Report on the Year 2001 Initiative found that qualified IT workers are a scarce resource. The demand for IT workers continues unabated, yet the number of students graduating with a bachelor's degrees in computer science continues to drop. Panelists from industry, academia, and policy groups will discuss their views on how to find and educate the geeks of the future.

MODERATOR
Caroline Wardle, NSF
PANELISTS
Cheryl Allan, Intel Corp.
Erich Bloch, The Washington Advisory Group
Anita Borg, Institute for Women and Technology/Xerox PARC
Peter Freeman, Georgia Tech

The Role of Java in High Performance Network Computing

This panel, which is sponsored by the Java Grande Forum, will review recent progress in the use of Java in high performance network computing. The Java Grande Forum (JGF) is an open forum with industrial, academic, and government participants motivated by the notion that Java could be the best possible development environment for "grande" applications. Grande applications are those demanding significant computing resources; they include classic high performance numerical computing such as fluid dynamics simulations, but also problems such as data mining and analysis, where large-scale I/O and network access is required. Java's potential is based on its high degree of portability, its network-aware environment, its vast array of utilities and services, and its widespread acceptance. There are now early signs that Java performance need not be lackluster: codes showing performance in the range of 50-90% of optimized Fortran or C have been demonstrated. Nevertheless, routine success for grande applications will only be realized if significant extensions to the Java language and platform are adopted.

The major goal of the JGF is to assess the status of Java for grande applications, to clearly articulate community requirements, and to provide proposals for extensions. The JGF has two major units: the Numerics Working Group and the Concurrency and Applications Working Group. The JGF and its working groups host open meetings and develop reports, benchmark suites, and prototype class libraries. The JGF Web page is at http://www.javagrande.org/. Panelists will briefly describe the current status of JGF activities and present several applications in which high performance computing and Java intersect.

MODERATORS
Ron Boisvert, NIST
Geoffrey Fox, Syracuse U.
PANELISTS
George Almasi, IBM
Denis Caromel, Institut National de Recherche en Informatique et en Automatique
Dennis Gannon, Indiana U.

Birds-of-a-Feather sessions, or BOFS, are informal get-togethers for conference attendees to discuss topics of mutual interest. Below are descriptions of BOFs that were scheduled at the time this program went to press. A BOF notice board with final dates, times, room numbers, and any additional sessions will be posted daily in the convention center.

Extensive RNA Secondary Structure Prediction Method Using Scalable Parallel Supercomputer IBM SP

Kenji Yamamoto, U. Toyko
bacteria@ims.u-tokya.ac.jp

An extensive RNA secondary structure prediction method using scalable parallel supercomputer IBM SP is reported. RNA secondary structures are closely related to a lot of biological aspects of virus activities. To investigate these activities, finding not only the optimal structures but also all the sub-optimal secondary structures is very important. Yamamoto et al. developed a search tree method finding all the sub-optimal secondary structures using 8-queen's approximation (Yamamoto et. al. 1984). However, search tree method with 8-queen's approximation is too demanding to evaluate a full-size RNA molecule of such as Poliovirus or HIV. We propose an extensive sweeping method with

a Windows approach to find almost all the possible sub-optimal secondary structures to the size of Poliovirus or HIV RNAs. Here, each sweep is algorithmically independent, so we parallelized this code with MPI on IBM-SP.

Grid Forum

Ian T. Foster, ANL and U. Chicago
foster@mcs.anl.gov

- The term "Computational Grid" refers to an infrastructure designed to support the coordinated use of diverse distributed resources: computers, storage, networks, scientific instruments, etc. Large national programs (e.g., the NSF PACIs, NASA IPG, DOE's DISCOM and NGI) are sponsoring R&D in this area and large-production Grids are being constructed. In the commercial arena, developments relating to Java, JINI, CORBA, etc., are also very relevant. In this context, the Grid Forum has been established to provide a focal point for information exchange and discussions relating to infrastructure, tools, standards, and best practices relating to Grids. To date, two meetings have been held, in June and October, nine working groups established, and working documents have been produced. This BOF will provide a unique opportunity for interested members of the SC conference community to learn about the activities of the Grid Forum and to participate in a discussion about its function and future.

High Speed Interconnects for COTS Cluster Computing

Markus Fischer
markus@markus-fischer.de

- Cluster Computing is one of the most important research platform for parallel computing in the recent years. With high volume production processors such as Intels PIII and now AMDs Athlon's CPU, high computation performance is available through these COTS at low costs. However, dense packing of processing units is easier than increasing the performance of IO. Therefore, the performance gap to communication and I/O in general is steadily increasing. While Gigabit/s media exist to transfer data, the current bottleneck is the interface between CPU and NIC. Improvement of main memory access, as well as inter node data transfer bus have been becoming a research platform lately (Rambus). Due to the availability of the PCI bus in most systems, network interface cards currently use this interface for communication, being limited by the 32/64 bits wide bus running at 33/66 Mhz, respectively. Approaches to overcome this scenario are Future IO and NG IO which have merged to SIO recently. However PCI (-X) systems will continue to exist for at about 3-5 years. High Speed Interconnects such as Myrinet, SCI and ATOLL are offering new programming paradigmas and each interconnect has it's advantages and drawbacks. An industry standard such as VIA has been specified, but first implementations already point out problems for its implementation and realisation. As a result of this BOF we expect to have a higher transparency of current high speed interconnects and their software environments, also pointing out the demands of software developers.

  Our speaker would first present results on:

  Topics:
  - 1) A comparison of high speed interconnects in the market: Myrinet, Servernet, SCI
  - 2) Software models such as MPI-1, MPI-2, PVM, VIA, with details on their NIC specific implementation including zero-copy, DMA copy / PIO
  - 3) Presentation of a new fully integrated high speed interconnect: ATOLL, a network on a chip

- 4) Early experiences in One sided communication in MPI-2
- 5) Experiences in implementing VIA

Information Technology for the 21st Century EPSCOR Roundtable

Barbara Kucera
mailto:bkucera@ncsa.uiuc.edu

- This BOF will include a presentation from NPACI and a presentation on two very important topics in Washington, DC, now - the President's Information Technology Advisory Council and Information Technology Research (PITAC/ITR). This will be followed by a roundtable discussion to see if a virtual, western states collaboration is possible. The Southeastern states, the New England states, and the Great Plain group have gotten together and are collaborating already; we hope to determine the level of interest for the western states forming such a group.

Large-scale PC Clusters: Issues, Solutions, and Partnerships

Jeffrey J. Nucciarone, Pennsylvania State University
nucci@cac.psu.edu

- The design of Intel's Pentium processor based PC Cluster, using low cost off-the-shelf technology, requires a delicate balance of performance, reliability, and expense. Traditionally most PC Clusters are designed and built by small research groups who trade higher availability and performance for lower cost. This contrasts with issues faced by a central computing facility where the job mix varies widely and is less predictable. The Pennsylvania State University's LION-X PC Cluster has been designed with the need to balance overall cost with the performance and reliability of a system expected to meet the requirements of serving a diverse group of researchers. Its high performance nodes and multiple high-speed data networks (Fast and Gigabit Ethernet, Myrinet) provide researchers with a powerful distributed memory parallel system. We wish to discuss what other large sites are implementing, what problems they may be encountering, and how to work together in this area.

Message Passing for Java

Vladimir Getov, University of Westminister
V.S.Getov@wmin.ac.uk

- This BOF session will serve as an open meeting of the Java Grande MessagePassing working group. The group is a community effort within the frame of the JavaGrande Forum activities. The aim of the group is to provide an environment for discussion and collaboration in the research and development of portable message-passing frameworks and corresponding APIs for the Java programming language with focus on JavaGrande applications. Important current objectives of the group are the development of an MPI-like API for Java - MPJ, research into O-O Java-centric message-passing environments, the development of a single strategy for the introduction of message passing into the Java platform, and performance evaluation and comparisons between different frameworks and implementations. The session will include (provisionally) short presentations from Bryan Carpenter, NPAC; Glenn Judd, BYU; Doug MacDonald/Eric Sharakan, Sun-HPC; Tony Skjellum, MST; and Marc Snir , IBM.

Myrinet Users Group

Nan Boden, Myricom Corporation
nan@myri.com

- Myrinet is a cost-effective, high-performance, packet communication and and switching technology widely used to interconnect clusters of computers. Myricom (www.myri.com) shipped the first Myrinet products in 1994. There are now approaching 1000 Myrinet installations worldwide, ranging in size from two to 1400 hosts. These sites include many of the world's premier cluster computing systems and many sites represented at SC99. Myricom, at the suggestion of our customers, is exploring the idea of sponsoring a Myrinet Users Group to further the development, applications, and software sharing for Myrinet clusters. The focus of this BOF session would be to solicit ideas for a Myrinet Users Group, and to discuss the present state of the art in Myrinet clusters and the future directions of Myrinet technology.

OpenMP: Past Success and Future Directions

Tim G. Mattson, Intel Corporation
tgmattso@ichips.intel.com

- OpenMP is an industry-wide application programming interface for writing programs for shared memory, parallel computers. It was created by a group of key hardware and software vendors to standardize common practice and to make portable, parallel programming a reality for shared memory systems. The first OpenMP specification was released in 1997 for Fortran77 with the C/C++ specification following in 1998. Currently, the OpenMP architecture review board (ARB) is working on version 2.0 of OpenMP, which will extend the standard to a wider range of applications and better meet the needs of Fortran95 programmers. This BOF will provide a first look at our continuing work on OpenMP version 2.0. It will also provide a forum for users of OpenMP to discuss their work with OpenMP. Finally, representatives of the OpenMP ARB will be on hand to field questions and take input on future directions for OpenMP.

Portable Batch System (PBS)

James Patton Jones, MRJ Technology Solutions
jjones@pbs.mrj.com

- MRJ invites all current and potential users of the Portable Batch System (PBS) to this Birds-of-a-Feather session. Come and meet PBS support and development staff. Hear about PBS v2.2 capabilities and features; learn about planned enhancements, and share your ideas and experiences with other PBS users. The Portable Batch System, developed at NASA Ames Research Center, is a POSIX-compliant batch queuing and resource management environment designed for high performance computers as well as MPPs and workstation clusters. PBS is Open Source software with commercial support available from MRJ.

Project HTMT Architecture for Petaflops Computing

Lawrence Picha, NASA
lpixa@jpl.nasa.gov

- An active community of research scientists is working toward the vision of Petaflops-scale computing-a performance level that may be feasible within the next five to seven years through a mix of emerging innovative device technologies. A Project (HTMT) is now actively pursuing recent and important advances in the fields of superconductor logic, optical communications and storage, and processor-in-memory (PIM) semiconductor fabrication that are yielding dramatic improvements in speed, power consumption, and parts count with respect to conventional device technologies. The HTMT Project developed the Hybrid-Technology Multithreaded (HTMT) parallel computer architecture, addressing the challenges of incorporating these new devices in effective computing systems. HTMT employs proactive latency management and parallel task scheduling mechanisms enabled by PIM DRAM and SRAM eliminating most long access delays and overhead operations by the very high speed processors, thus providing high processor efficiency. All interested in this research activity are invited to attend.

SC2000 Education Program

Jeffrey Huskamp
HuskampJ@mail.ecu.edu

- The SC2000 Education Program committee is looking for input, and your ideas are encouraged during this BOF. SC2000 will offer high school teachers an opportunity to participate in the SC2000 Educational Leadership Program to earn computer modeling and simulation techniques and their application to the science and mathematics curricula. Researchers, scientists, and educators who have experience in implementing computational science and visualization programs for undergraduates and graduate students as well as high school teacher participants are strongly encouraged to share their experiences through submitted papers and focused panels.

Technology Transfer for High Performance Computing

Ron H. Perrott, University of Queens-Belfast; Margaret Simmons, NPACI/SDSC
R.perrott@qub.ac.uk

- For several decades, universities and research institutions have developed and refined the use and application of HPNC, particularly, in science and engineering applications. However this technology has yet to achieve widespread penetration in the industrial and commercial sectors. One of the reasons for this lack of take up is the lack of a technology transfer effort targeted at companies that are traditionally conservative in their approach to computing. This BOF session will consider efforts in progress that are promoting technology transfer in Europe, US and elsewhere and consider what should be done in the future to promote and enhance the widespread use of HPCN in the non-university sectors.

The IEEE Task Force on Cluster Computing

Tim G. Mattson, Intel Corporation
tgmattso@ichips.intel.com

- Computing with clusters of computers has been around for a few decades. Recently, however, it has become a hot technology with cluster products emerging across the world of computing. But what exactly is a cluster? What are they used for? How should a programmer write software that can take advantage of a cluster? In 1999, the IEEE Task Force on Cluster Computing was formed to address these and other cluster computing issues. You can learn more about the task force at http://www.dcs.port.ac.uk/~mab/tfcc/. At this BOF, we will introduce the task force and lay out our strategy for advancing the impact of cluster computing. Representatives from a diverse range of cluster computing interests will present their views on clusters and lead what are expected to be lively discussions.

The Parallel Tools Consortium (Ptools)

Judith Ingles
jingles@us.ibm.com

- A national task force was convened to determine what types of system software and tools were sufficiently important to warrant implementation across multiple vendors and machine types. The goal was to develop guidelines for including system software and tools in procurements for HPC systems. This was a collaborative effort involving both users and developers of HPC software. The effort was focused into several meetings, each involving a different set of participants from distinct sectors of the HPC community. The discussion will explore the issues of requirements and procurements. The panel will include representatives the user community and developers of HPC software.

  The Task Force is endorsed by the Parallel Tools Consortium and the National Coordination Office for Computing, Information, and Communication. Financial sponsorship was supplied through an interagency grant. wide variety of platforms.

TOP500 Supercomputers

Erich Strohmaier, U. Tennessee, Knoxville
erich@cs.utk.edu

- The TOP500 report is a snapshot of the state of supercomputer installations in the world. It is based on the TOP500 list that will be published in November 1999 and includes trends from the previous lists of 1993-1999. Statistics on high performance computers are of major interest to manufacturers, users, potential users, and decision makers in universities, government, and industry. These people wish to know not only the number of systems installed, but also the locations of the various supercomputers within the high performance computing community and also the applications for which a computer system is used. Such statistics provide a better understanding of the high performance market and can facilitate the exchange of data and software. This report is meant as an interface between the TOP500 list and the reader who wishes more background information and explanation. Here various experts present detailed analyses of the TOP500 and discuss the changes that have been made.

Using Clusters for Visualization

Arthurine Breckenridge, Sandia National Laboratories
arbreck@sandia.gov

- Scientific visualization has long been used as an analysis tool for modeling and simulation. As many ultracomputers are now based on cluster technologies, it is appropriate to apply this scalable architecture to visualization. The BOF will bring together individuals working in parallel processing and rendering of very large datasets.

Valuation of Ultra-scale Computers

Ian T. Foster, ANL and U. Chicago
foster@mcs.anl.gov

- Ensuring that Ultra-scale (multi-Teraflop/s) supercomputers are available for scientific applications requires considerable public investment in infrastructure. The effective and efficient use of public resources to build this infrastructure is frequently questioned. It is difficult to adequately answer these questions by accurately describing the value of such unique, and often experimental, computing resources. Generally, valuation metrics such as total CPU utilization, time to solution, quality of the resulting "science" is proposed. Over the last few months representatives of government agencies, laboratories, and the academic community have discussed various valuation metrics, techniques for measuring "value" and ways of improving utilization. The results of an October Summit on Ultra-scale Computing Valuation will be highlighted and discussed at this BOF. Come and participate in a valuable information exchange and discussion.

This year's Education Program will offer the teacher who feels challenged with the rapid evolution of information technology an opportunity to share information with peer groups and to learn what is actually working and how it is being used in the classroom. We will also explore strategies to attract more students to technology-especially students from underrepresented groups.

Birds of a Feather Breakout Sessions

- Select one of six sessions to attend: Math, Media/Library, Special Needs/At Risk, Science, Programming, or Networking. Facilitators will lead the groups through the process of sharing information on what is working and how technology integration has been accomplished in the classroom.

Careers in Technology

Panel Discussion of Industry Leaders

- The panel will discuss information that teachers need to know to help inform students about careers in technology, including the role of education in helping students prepare for future employment. This session will also help bridge the gap between what teachers are sharing with students and the current needs of industry.

Ethernet a la Carte

Evan McConnell, EarthWalk Communications, Inc.

- A valuable hands-on demonstration of a wireless classroom that will include information on how to create up to a 32-unit lab without having to rewire or add additional electrical power. Participants will be able to use the computer lab on wheels during this presentation and discuss the future of wireless systems for classrooms.

Exhibitor Round-Robin Sessions

- Participants will be able to attend three 30-minute sessions being presented from selected SC99 industry and research exhibitors about their education programs. These exhibitors will give you the opportunity to discuss the programs being developed and how you can make the link between education and the workforce. What do you need to do in the K-12 education system to enhance the preparation of your students for their futures?

LINUX Classroom Applications

Paul Nelson, Riverdale School District Oregon

- Can free software really be this good? LINUX is a free operating system that is making inroads into the server market. The next target is the desktop. See what it can do for your schools as a cross-platform server and general-use desktop OS. School applications will be demonstrated and hands-on activities will provide the user with an opportunity to experience a different operating system.

Preview Panel on Strategies for Student Recruitment in Math, Science, and Technology

Moderator: Mary Bunn, Oregon Department of Education

- A preview of the organizations that will be presenting strategies for student recruitment at 10:30am; this will enable teachers to choose which breakout sessions to attend. Representatives of these organizations will briefly introduce themselves and tell teachers what to expect if they choose to attend their session.

SC2000 Education Program

November 04-10, 2000
Dallas, TX
education@SC2000.org
http://www.sc2000.org/education

- Teachers: it's not too early to consider participating in SC2000!

  SC2000 offers high school teachers an opportunity to participate in the SC2000 Educational Leadership Program to learn computer modeling and simulation techniques and their application to the science and mathematics curricula. Researchers, scientists, and educators who have experience in

implementing computational science and visualization programs for undergraduates and graduate students as well as high school teacher participants are strongly encouraged to share their experiences through submitted papers and focused panels. After the conference, the high school teachers will receive ongoing support from SC2000 staff to assist in adopting what they have learned to the classroom. The teachers participating in SC2000 will be expected to be leaders in their school systems for a wider adoption of modeling and simulation by additional teachers. Then, at SC2001, selected teachers will share their experiences during the year with other teachers. Applications can be made from the SC2000 Web page.

Strategies for Student Recruitment in Math, Science, and Technology

Mary Bunn, Oregon Department of Education

- Attendees will be able to select up to three interactive 30-minute sessions conducted by representatives from organizations working to involve young women and other under-represented populations into mathematics, science and technology. Breakout presenters will provide strategies for recruitment and retention and information about lessons learned in working with these targeted populations.

The Future of Computing

Thomas Jones, Chemeketa Community College

- Crystal ball not working for you? This session will give you a look at the future of technology in a humorous way.

Training the Next Generation of Network Administrators

Don Wolff, Phoenix-Talent School District

- Routers, patch cables, punch-down blocks, and RJ-45 jacks: not your ordinary list of back-to-school supplies. Then again, for students across the country in a unique new curriculum known as the Cisco Networking Academy, the fall semester was anything but your ordinary back-to-school experience. In a lab setting that closely corresponds to the real world, students get hands-on experience with the building blocks of today's global information networks. This session will provide you with information about the curriculum and how you, too, can get started.

Vernier Software-Data Collection in the Classroom

Rick Sorensen, Vernier Software

- Learn how you can use Vernier software with equipment to collect and analyze data in your science or math class. This software and equipment can be used with computers in the classroom or taken into the field. With Vernier sensors like the Motion Detector, your students can study free fall, terminal velocity, and collisions. With sensors like a Dissolved Oxygen Sensor, students can investigate water quality in nearby streams or lakes. Students can use a Biology Gas Pressure Sensor or Carbon Dioxide

Gas Sensor to measure plant transpiration. A complete array of sensors provides many data-collection opportunities. Computer software simplifies data collection with computers and provides extensive analysis tools. Support for graphing calculators provides even more flexibility. Take a hands-on look at this sampling of educational technology.

Vision of K-12 Technology from the State Superintendent Viewpoint

Stan Bunn, Oregon Superintendent of Public Instruction

- Educational Reform is occurring in all states. How does technology support these initiatives and how is it being implemented in Oregon? What are the expectations of using technology as a tool as it is integrated into the curriculum?

Voice Recognition

Ronald A. Cole, Center for Spoken Language Understanding, U. Colorado

- This session will give attendees an opportunity to learn the basics of how technology and voice recognition software work. Find out what applications are available or being developed and how they may fit into your school. Each attendee will receive a Spoken Language Understanding Tool Kit.

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Last Modified: Sep 25 1999

Abstracts for each research exhibit, including the exhibitor's url(s) and in some cases a highlighted demonstration are given below in alphabetical order by exhibitor name.

- Institut National de Recherche en Informatique et en Automatique (INRIA)
- Institute for Software Technology and Parallel Systems, University of Vienna, Austria: Advanced Symbolic Debugging of HPF Programs with SPiDER
- Internet2
- Japan Marine Science and Technology Center (JAMSTEC): Earth Simulator Project and STA HPC Group
- Japan Science and Technology Cooperation (JST): JST Super Computer Complex
- Krell Institute: Computational Science Programs at the Krell Institute
- Los Alamos National Laboratory
- Maui High Performance Computing Center and Albuquerque High Performance Computing Center
- NASA Jet Propulsion Laboratory/California Institute of Technology Project HTMT: Hybrid Technology Multi-threaded -class Architecture for Petaflops Scale Computation
- National Aeronautics and Space Administration
- National Aerospace Laboratory of Japan and STA HPC Group
- National Center for Atmospheric Research - Scientific Computing Division: The Virtual Earth System
- National Center for High-Performance Computing (NCHC): High Performance Computing and Networking in NCHC, Taiwan
- National Computational Science Alliance
- National Coordination Office for Computing, Information, and Communications
- National Partnership for Advanced Computational Infrastructure (NPACI)
- NOAA/FSL Realtime Weather Forecasting
- North Carolina Supercomputing Center
- Northwest Alliance for Computational Science and Engineering: Tools for Exploration of Scientific Data
- Oak Ridge National Laboratory
- Ohio Supercomputer Center: Computing and Networking for the People
- Pacific Northwest National Laboratory (PNNL): Science Through Computational Science at PNNL
- Parallel Tools Consortium
- Pittsburgh Supercomputing Center
- Purdue University / Standard Performance Evaluation Corporation: Benchmarking for High-Performance Computing
- Real World Computing Partnership: Toward Seamless Parallel and Distributed Computing at RWCP
- Research Center Juelich: Distributed Computing in Heterogeneous Supercomputer Environments
- Research Organization for Information Science & Technology
- Saitama University: Scientific Computing and Visualization and Their Applications for Education
- SC2000

- **SC99 Research Exhibit Committee**
- **SCinet99**
- **The Aggregate**
- **The Institute of Physical and Chemical Research (RIKEN): 13 Tflops Special-purpose Computer for Molecular Dynamics Simulations**
- **The MITRE Corporation**
- **The National Center for Data Mining and The National Scalable Cluster Project: Technologies for Mining and Modeling Massive and Distributed Data**
- **Universidade de Sao Paulo: SPADE-II System and High Performance Applications**
- **University of California, Berkeley -- Millennium Project**
- **University of Greenwich: Computer Aided Parallelisation Tools (CAPTools)**
- **University of Manchester: Manchester Computing**
- **University of Tokyo: GRAPE-5 and GRAPE-6: Special-purpose computers for Astrophysical N-body problem**
- **University of Virginia: Legion - A Worldwide Virtual Computer**
- **Waseda University: Parallel and Distributed Computing Environment**

Ames Laboratory: Gigabit Ethernet in Scalable Computing Applications

http://www.scl.ameslab.gov
http://www.scl.ameslab.gov/SC99

Abstract:

The SCL will present in-depth results from several high performance cluster computers employing Gigabit Ethernet as their message-passing communication fabric. Through the utilization of large packet frames, OS bypass research, and light weight message-passing protocols, we will illustrate the price performance benefit of extending the Ethernet standard for cluster computing. Through our aggressive industrial partnership program, we have secured a joint research effort with IBM corporation and several Gigabit Ethernet vendors targeted at verify the applicability of cluster computing for real-world scientific applications. These collaborations have lead to Gigabit Ethernet yielding single stream throughputs in excess of 100MegaBytes/second. Our research covers cluster design, benchmarking, and configuration issues with particular regard to using commodity components to produce a scalable solution that is easy to construct, maintain, and upgrade. We also address the issue of providing a truly parallel aware batch scheduler to run in production code environments.

Highlight:

The Scalable Computing Laboratory in the DOE Ames Laboratory will be demonstrating high-speed network communications using Gigabit Ethernet, Jumbo Frames, and OS bypass techniques on high-end SMP systems. The throughput from this Power3 IBM workstation cluster presents the clear price performance benefits of commodity networking over custom-built interconnects.

Argonne National Laboratory

http://www.mcs.anl.gov

- Abstract:

  Researchers at Argonne National Laboratory provide information technology for today and for the future. The exhibit showcases current work in the following areas:

  - Numerical tools and libraries for large-scale computational applications ADIC, ADIFOR, ALICE, and PETSc.
  - MPI-2 and tools for parallel computing MPICH, Nupshot/Upshot and ROMIO
  - Collaborative tools and immersive visualization ManyWorlds, Metro and Voyager.
  - NGI advanced networking and ultra-LINUX clustering.
  - Advanced visualization environments featuring the Active Mural multiresolution display.
  - The GlobusProject: to develop the software infrastructure for management of the national computational grid.
  - The Optimization Technology Center and the NEOS Server, providing access to the latest optimization techniques over the Internet.
  - Associated scientific computing applications in combustion, computational chemistry and structural genomics.

  Closely tied with these projects will be an emphasis on collaborations with the ASCI program, CRPC, the DOE2000 program, the NCSA PACI Alliance, and the Scalable I/O Project

Arctic Region Supercomputing Center

http://www.arsc.edu/
http://www.arsc.edu/pubs/SC99/

- Abstract:

  The Arctic Region Supercomputing Center supports the computational needs of researchers within the Department of Defense, the University of Alaska Fairbanks, and other academic institutions and government agencies by providing high performance networking and computing resources, programming and technical expertise, and training. Areas of specialty supported by ARSC include ocean modeling, atmospheric sciences, climate/global change, space physics, satellite remote sensing, and civil, environmental, and petroleum engineering. The Arctic Region Supercomputing Center operates a Cray T3E and a Cray J932,with visualization resources including a Pyramid Systems ImmersaDesk and a network of SGI workstations located in a video production/training lab and three additional access labs on campus.

- Highlight:

  Spatially distributed Coupled Hydrologic and Thermal Processes. A 3-D model links surface/subsurface thermal and hydrologic processes yielding information on soil moisture, surface runoff, evaporation, snowmelt, and active layer development in Alaska. Seismic Wave Propagation: The 3-D visualization portrays propagation of seismic waves through the Earth from an earthquake occurring in a subducting slab beneath Alaska.

Berkeley National Laboratory (Ernest Orlando Lawrence Berkeley National Laboratory)

http://www.lbl.gov
http://www.nersc.gov
http://www.es.net

- Abstract:

  Berkeley Lab Computing Sciences is home to the U.S. Department of Energy's National Energy Research Scientific Computing Center (NERSC) and the Energy Sciences Network (ESnet). Since 1974, NERSC and ESnet have pioneered the field of high-speed remote access to supercomputers and have served as a model for other facilities. Our display will showcase both and illustrate our history and contributions over the past 25 years, as well as provide demonstrations of the latest advances in scientific computing.

- Highlight:

  Distributed IBR-Assisted Volume Rendering. As part of its work on the Next Generation Internet, Berkeley Lab will demonstrate remote volume rendering of combustion accelerated by employing a lazy evaluation of the plenoptic function using methods from image-based rendering (IBR). This results in a technique that can scale gracefully with volume size and network bandwidth.

Boston University

- Abstract:

  Boston University's research exhibit features its NSF-funded project, MARINER: Mid-level Alliance Resource In the North East Region. MARINER is a partner in the National Computational Science Alliance and extends the university's efforts in advanced scientific computing and networking to organizations throughout the region. Demonstrations of current research and educational projects developed through the Center for Computational Science and the Scientific Computing and Visualization Group will be shown using graphics workstations and videos in the exhibit booth. In addition, we will present distributed supercomputing applications, video animations of recent research, and 3-D visualizations using immersive displays.

Brookhaven National Laboratory: High Performance Scientific Computing at Brookhaven National Laboratory

http://www.bnl.gov
http://www.ccd.bnl.gov/visualization/

- Abstract:

  Brookhaven National Laboratory, a US Department of Energy multi-program laboratory, provides leading-edge, user-oriented scientific facilities and conducts basic and applied research. We exhibit high performance computing efforts which support our scientific focus:

  - *Stereoscopic Scientific Visualization*. A high-resolution, portable, stereoscopic projection system demonstrates complex scientific visualizations in computed microtomography, nuclear physics, and atmospheric aerosol models.
    http://www.ccd.bnl.gov/visualization/
  - *Relativistic Heavy Ion Collider (RHIC)*. RHIC experiments investigate conditions believed to have existed immediately after the Big Bang. We highlight state of the art computational

facilities for recording and analyzing petabytes of experimental data.
http://www.rhic.bnl.gov/

- *Center for Data Intensive Computing (CDIC)*. We highlight CDIC's impact on programs in high-energy and nuclear physics, aerosol and climate studies, combustion chemistry and cancer therapy treatment planning.
http://www.cdic.bnl.gov/
- *RIKEN-BNL Research Center Supercomputer*. RIKEN-BNL Research Center and Columbia University have built a 12,228 node, .6 Teraflop supercomputer. We showcase performance and results for quantum chromodynamics and other physics applications.
http://www.ccd.bnl.gov/riken_bnl/

- Highlight:

  Big Bang Theory Investigated at BNL. Experiments at the RHIC facility will attempt to create a form of matter that has not existed since moments after the Big Bang. See our stereo visualization of what a rare state of matter might look like shortly after the creation of the universe.

Center for Advanced Computing Research, California Institute of Technology

http://www.cacr.caltech.edu

- Abstract

  The Center for Advanced Computing Research (CACR) at the California Institute of Technology was established to foster advances in computational science and engineering. Therefore, CACR focuses on enabling breakthroughs in computational science and engineering by:

  - following an applications-driven approach to computational science and engineering research,
  - conducting multidisciplinary research on leading-edge computing facilities,
  - providing a rich, creative intellectual environment that cultivates multi-disciplinary collaborations, and
  - harnessing new technologies to create innovative large-scale computing environments.

  To achieve these goals, CACR conducts multidisciplinary, application-driven research in computational science and engineering through collaborations with Caltech and JPL faculty and staff and research and developments throughout the world. Results from these collaborations will be featured in the research exhibit.

Center for Promotion of Computational Science and Engineering (CCSE) at Japan Atomic Energy Research: R&D Activities on Parallel Processing Engineering

http://guide.tokai.jaeri.go.jp/ccse/

- Abstract:

  CCSE of Japan Atomic Energy Research Institute was formed in April 1995 by governmental guidance to promote computational science and engineering among the national and other semi-governmental research organizations.CCSE has the best equipped complex parallel computer system consisting of nine sets of different types of parallel computers. CCSE has put special emphasis on the R&D activities of parallel computing technologies and developed a common technological

basis of parallel processing technologies such as

- parallel basic software,
- parallel computational algorithms,
- parallel processing tools, and

as a specific application of these technologies,

- the development of techniques for numerical experiments.

- Highlight:

  CCSE will demonstrate Seamless Thinking Aid software (which supports a distributed parallel, metacomputing environment), a parallel numerical library (including linear equation solver, random number generator, FFT, etc.), real-time visualization software, mesh generation, a parallel performance measurement tool, and large-scale numerical simulation results.

Center for Supercomputing Research and Development (CSRD) --- University of Illinois at Urbana-Champaign

http://www.csrd.uiuc.edu/
http://www.csrd.uiuc.edu/promis

- Abstract:

  CSRD has been a prominent leader in the high-performance computing community. Our exhibit presents the following four major projects on parallelizing and optimizing compilers, user-level thread models, runtime environments, and multithreading architectures:

  - The PROMIS Compiler aims at synergistic exploitation of inter- and intra-processor parallelism and features an integrated frontend and backend operating on a unified internal representation. Symbolic and pointer analyses are used in conjunction with other analysis and transformation techniques to aggressively optimize programs.
  - Server significantly improves JAVA virtual machine scaling and performance. A non-blocking scheduler reduces parallel access overhead and decreases overall system design complexity. Multiprogramming extensions allow the VM to reuse data and code across multiple users.
  - The Illinois-Intel Multithreading Library offers a unified support for structured, unstructured, and nested parallelism without sacrificing performance of parallel loops.
  - a-Coral is a multithreaded out-of-order superscalar architecture aiming at hiding branch and memory latency.

- Highlight:

  The CSRD booth features the PROMIS compiler demonstration. PROMIS is a multilingual, retargetable, parallelizing, and optimizing compiler under development. Through the PROMIS GUI, we illustrate the analysis, parallelization and optimization of several standard benchmark programs (written in FORTRAN, C, C++, and JAVA).

CHPC, University of Utah: High Performance Computing at the University of Utah

http://www.chpc.utah.edu
http://www.chpc..utah.edu/sc99

- Abstract:

  The Center for High Performance Computing provides large-scale computer resources to facilitate advances in the field of computational science at the University of Utah. The projects supported by CHPC come from a wide array of disciplines requiring large capacity computing resources, both for calculating the solutions of large-scale, 2-and 3-D problems and for graphical visualization of the results.

- Highlight:

  The Center for Scientific Computing and Imaging is actively involved in scientific computing and visualization research with a focus in the areas of problem-solving environments, scientific visualization, computational steering and interactive scientific computing, numerical methods, and parallel computing. We are applying our research to application areas such as computational medicine, inverse and imaging problems, computational fluid dynamics and combustion, and geoscience.

CLRC: Computational Science and Engineering at CLRC

http://www.cse.clrc.ac.uk/

- Abstract:

  The Computational Science and Engineering Department at CLRC acts as a UK focus for the development, application, and support of research in computational science and engineering. We will overview our work with the UK academic community, focusing in particular on scientific highlights from the collaborative computational projects and our high performance computing activities, including high performance quantum chemistry applications, modeling mechanisms for DNA fragment transport across cell membranes, first principles molecular dynamics simulations of water adsorption on oxide surfaces, modeling high- temperature superconducting properties, Reynolds stress laminar flamelet models of turbulent pre-mixed combustion, parallelization of FLITE3D-an irregular grid whole aircraft Euler solver, PARASOL: an integrated environment for parallel sparse matrix solvers, and Computers by Design-virtual benchmarking of parallel systems in real applications.

Department of Defense High Performance Computing Modernization Office (Program)

http://www.hpcmo.hpc.mil

- Abstract:

  The High Performance Computing Modernization Office (HPCMO) will demonstrate its support to the DoD and the warfighter via a multimedia CDROM, an interactive poster slide show and some limited demonstrations. We will emphasize how the technology employed by the High Performance Computing Modernization Program "trickles down" to help the warfighter. We will show the Computational Technology Areas supported by the program, where these areas are supported, and highlight some of the "Challenge Projects" for the past year. We will also describe t

Since time immemorial, men and women have tested themselves with feats of physical prowess. They have raced by foot and chariot. They have lifted great weights. They have climbed mountains and swum rivers. Olympic exhibitions of athletic skill, grace, and beauty thrill have thrilled the human soul.

Today, we hack code. That's what the HPC Games are about.

This year several teams will come together to show off their computing skill, grace, and beauty. They come from around the world to demonstrate the cool stuff they can do on high performance machines. They fight for a moment of glory at the Thursday afternoon awards session and a stack of free t-shirts.

The teams compete by giving demonstrations on the research exhibit floor on Wednesday afternoon. Demos will run from 2-4pm that day; a complete schedule will be available at the entrance to the exhibits hall. The teams choose their own problem to solve, ranging from solid state physics to the state of the universe. A team of expert judges will rate them on three criteria:

- Speed: The traditional measure of high performance computing, operations per second.
- Distance: The less traditional measure of distributed computing, great circle distance between processors used in the computation.
- Style: Audience applause will sway the judges.

Although prizes will be given, the real purpose of the HPC Games is to have fun and show off new ideas. This event continues the tradition of the HPC Challenge, a popular showcase in previous years.

HPC Games Chair: Charles Koelbel, National Science Foundation
Vice-Chair: Eleanor Anne Schroeder, Naval Oceanographic Office

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Last Modified: Sep 4 1999

- Posters are listed alphabetically by last name of presenter (name underlined).

- UPS: Unified Parallel Software - Richard F. Barrett, Mike McKay Jr and Sunlung Suen.
- ICEPIC: A 3-D Parallel Particle-in-cell Code - Joseph D. Blahovec, Lester A. Bowers, John W. Luginsland, Gerald E. Sasser, Shari L. Colella, Gerald E. Sasser and John J. Watrous.
- ARDRA, Scalable Parallel Code System to Perform Neutron and Radiation Transport Calculations - Peter N. Brown, Chang Britton, Keith Grand, Ulf R. Hanebutte, Carol S. Woodward and Thomas A. Brunner.
- Empirical Performance Modeling Using Synthetically Built Assemble Directives (SynBAD) - Kirk W. Cameron.
- An "HPspmd" Programming Model - Bryan Carpenter.
- Video killed the radio stars - Jean-Luc Dekeyser and Philippe Marquet.
- HDF5: A file format and i/o library for high performance computing applications - Mike Folk, Albert Cheng and Kim Yates.
- An Analysis of Performance Coupling Characteristics of High Performance Benchmarks - Jonathan G. Geisler.
- User Application Benchmarks for Beowulf Clusters and Conventional HPC Platforms - Jim Giuliani, David Heisterberg and Doug Johnson.
- Supercomputing with Cobalt - Matt Grismer, Ken Wurtzler, William Strang and Robert Tomaro
- Cluster Performance: SMP versus Uniprocessor Nodes - John L. Gustafson, Don Heller, Rajat Todi and Jenwei Hsieh
- Flexible Control Structures for Parallel C/C++ - Grant Haab, Sanjiv Shah, Paul Petersen and Joe Throop.
- High Performance Knowledge Discovery and Data Mining Systems Using Workstation Clusters - William H. Hsu, Michel Welge, Thomas Redman, Loretta Auvil and David Tcheng.
- The Vector, Signal, and Image Processing Library (VSIPL) Standard for High Performance Computing: Interface and Product Status of v1.0 - Jeremy Kepner, James Lebak, Randy Janka and Mark Richards.
- Dynamic Mesh Partitioning for Distributed Systems - Zhiling Lan, Valerie Taylor, Jian Chen and Gregory Bryan.
- Dual-level Parallelism Improves Load-Balance in the Production Engineering Application CH3D-SED. - Phu V. Luong, Clay P. Breshears and Henry Gabb.
- Parallel Models of Self-organized Criticality for Plasma Confinement - Vickie Lynch and Benjamin A. Carrereas.
- How to Schedule Parallel I/O Intensive Jobs - Jens Mache, Virginia Lo and Sharad Garg.

- Omega3P: Modeling Particle Accelerators With Greater Speed and Accuracy - Brian McCandless, Nate Folwell, Zenghai Li, Yong Sun and Kwok Ko.
- A Survey on Parallel Architectural Considerations and Databases - Edward D. Moreno, Marcos L. Mucheroni and Sergio T. Kofuji.
- PC Clusters for a Central Computing Facility: Design, Implementation, and Results - Jeffrey J. Nucciarone.
- EIGER -- Electromagnetic Interactions GenERalized - Robert M. Sharpe, Nathan J. Champagne, Kim Mish, Donald R. Wilton, John Rockaway, Charles Manry, William Johnson and Roy Jorgensen
- Ray Casting on a Shared Memory Multithreaded Supercomputer: Putting the Universe in Perspective - Allan Snavely, Greg Johnson and Jon Genetti.
- PSPARSLIB: A Case Study of a Resource-aware Parallel Linear System Solution - Masha Sosonkina and Yousef Saad.
- SCMS: An Extensible Cluster Management Tool for Beowulf - Putchong Uthayopas and Arnon Rungswang
- ScaleME: A Portable Distributed Memory Multilevel Fast Multipole Kernel for Electromagnetic and Acoustic Integral Equation Solvers. - Sanjay Velamparambil, Jiming Song and Weng Cho Chew.
- Performance of the Parallel Climate Model (PCM) on Various Architectures - Vince Wayland, Tom Bettge, Tony Craig and Rodney James.
- Intersim-VW: Scalable Visualizations of Internet Traffic Simulations - Martin D. Westhead.

UPS: Unified Parallel Software

Richard F. Barrett, Mike McKay Jr. and Sunlung Suen, LANL.

Poster URL: http://www-xdiv.lanl.gov/XCI/PROJECTS/UPS

- Abstract

UPS, an acronym for "Unified Parallel Software," is a library of routines designed to help the application developer create efficient, extensible, and robust large-scale parallel programs for physics simulations. It is designed to run in any computing environment that supports the C programming language and which provides a method for moving data between parallel processes. Our poster will describe how UPS is being used by several ASCI codes at Los Alamos National Laboratory. In addition to programming convenience, significant performance gains are realized by our users. We include graphs showing the performance of UPS on ASCI Blue Mountain.

ICEPIC: A 3-D Parallel Particle-In-Cell Code

Joseph D Blahovec, Lester A. Bowers, John W. Luginsland and Gerald E. Sasser, Air Force Research Laboratory
Shari L. Colella and John J. Watrous

- Abstract

ICEPIC (Improved Concurrent Electromagnetic Particle In Cell), developed at the Air Force Research Laboratory, is a 3-D particle-in-cell (PIC) code specifically designed for parallel HPC resources. ICEPIC simulates collisionless plasma physics phenomena on a Cartesian grid. ICEPIC has several novel features that allow efficient use of parallel architectures, including automated partitioning, dynamic load balancing, and an advanced parallel PIC algorithm. It is written in ANSI C to provide

portability to a variety of HPC systems. ICEPIC also contains 'intelligent' input file error checking and an automated test suite to ensure user friendliness and simplify its maintenance. Current challenges for ICEPIC development include MPI/PVM wrapper rewrite and the MPI vs. MPI/OpenMP hybrid issue.

ARDRA, Scalable parallel code system to perform neutron and radiation transport calculations

Peter N. Brown and Chang Britton- Center for Applied Scientific Computing, Lawrence Livermore National Laboratory
Keith Grand, Lawrence Livermore National Laboratory
Ulf R. Hanebutte and Carol S. Woodward, Center for Applied Scientific Computing, Lawrence Livermore National Laboratory
Thomas A. Brunner, University of Michigan.

Poster URL: http://www.llnl.gov/casc/Ardra/

- Abstract

The ability to model the transport of neutral particles such as neutrons and photons through matter is of importance to many scientific and engineering activities. In this work we present a scalable, parallel code system to perform neutral particle transport calculations in three dimensions. Ardra offers robust scalable solution methods for neutron and radiation transport problems in complex 3-D geometries. High resolution in space, energy and direction are supported. Ardra has demonstrated its capability to solve systems with billions of unknowns on terascale computers with 1000's of processors. The code's capabilities are demonstrated by a shielding calculation, which contains over 14 billion unknowns. To adequately resolve the spatial scale, which varies by 4 orders of magnitude, a spatial mesh of 536x540x552 mesh points (160 million zones) was selected. The neutron energy is discretized in 23 energy groups. Material properties in the calculation vary by 14 orders of magnitude.

Empirical Performance Modeling Using Synthetically Built Assemble Directives (SynBAD)

Kirk W. Cameron, Los Alamos National Laboratory

Poster URL: http://www.c3.lanl.gov/~kirk/isca99/

- Abstract

For computationally bound problems on parallel machines, single processor performance is often the bottleneck. According to Hennesy and Patterson in "Computer Architecture: A Quantitative Approach," on-chip processor performance loss after memory latency is primarily due to the mismatch between instruction-mix and static functional unit allocation. For this reason, we present a study of instruction-mix performance degradation in the context of empirical modeling based on elementary queuing theory. In particular, along with evaluating instruction-mix pattern influence on the MIPS R10000, we seek to qualitatively categorize dependence influence on performance. SynBAD, Synthetically Built Assemble Directives, is a tool providing for the manipulation of instruction and dependence mix patterns at the assemble level. Elements of SynBAD are portable and implemented on the MIPS R10000 using its on-chip hardware performance monitors for measurements and validation. We present SynBAD and results as they pertain to empirical modeling of single processor performance.

An "HPspmd" Programming Model

Bryan Carpenter, Syracuse University

Poster URL: http://www.npac.syr.edu/projects/pcrc/HPJava/

- Abstract

We motivate and discusses some features of a language model combining data-parallel features from HPF with an explicitly MIMD (SPMD) programming style. This model, which we call the "HPspmd" model, is designed to facilitate calls to libraries for parallel programming with distributed data. The slow uptake of HPF is partly attributed to immaturity in current compilers. But it seems that some programmers are equally comfortable with the explicit SPMD programming style. Many higher-level parallel programming environments and libraries assume this style (ScaLAPACK, PetSc, Kelp, the Global Arrays, etc). Unfortunately the library-based SPMD approach lacks the uniformity and elegance of HPF. The class of programming languages we discuss borrow ideas from HPF, but relinquish other principles. An explicitly MIMD programming model is complemented by syntax for representing distributed arrays. These features can make calls to various data-parallel libraries about as convenient as calling an array intrinsic function in Fortran 90.

Video killed the radio stars

Jean-Luc Dekeyser and Philippe Marquet, LIFL, University of Lille, France

- Abstract

Workstation capacities offer the chance to forget textual programming languages. If visual languages are often more difficult to learn and to use than Fortran-like languages, the association of the data-parallel paradigm and visual specifications open the access to parallel machines to a huge community of programmers. Gaspard is a graphical environment dedicated to an interactive and visual specification of dependencies between arrays and element array. The order of execution of SPMD tasks on array elements is automatically derived from the explicit dependencies. The compiler is able to extract two kinds of parallelism: task level according to the graph of the program, and pattern level according to the mapping iterator. Only SPMD tasks are textual. This environment is composed of a visual editor, a syntactic analyzer of the specifications, a code transformer, and a code generator for SMP computers.

HDF5: A file format and i/o library for high performance computing applications

Mike Folk and Albert Cheng, University of Illinois
Kim Yates, Lawrence Livermore National Laboratory

Poster URL: http://hdf.ncsa.uiuc.edu/HDF5/

- Abstract

The Hierarchical Data Format (HDF) has been used for scientific data management since 1988. HDF is used in many disciplines and supported by public and commercial software. NCSA is collaborating with NASA, the ASCI project, and others to provide a new format and library, HDF5, which addresses the needs of vastly expanded computational and storage systems, including massively parallel systems. The HDF5 data model is simpler and more powerful than the existing HDF4 data model. HDF5 offers improved performance by providing storage options such as data compression and tiling. Applications that drive HDF5 include applications on the ASCI "teraflops" machines, Earth science data management, and product model data exchange. I/O performance testing and tuning plays a critical role in the HDF5 project, particularly on I/O-intensive platforms, such as the ASCI machines. The poster provides details on the results of these activities.

The SC99 Industry Exhibits complement the technical program and feature industry leaders in HPNC and associated software, visualization, tools, storage, applications, and services. This exhibition is one you will not want to miss! It begins with a Gala Opening on Monday night and continues through Thursday of SC99.

ADIC
Booth 704
800-336-1233
amy.roy@adic.com
www.adic.com

ADIC (Advanced Digital Information Corporation) provides the industry's broadest range of automated tape systems for data storage and retrieval-from 7 tapes to more than 70,000-available with your choice of leading tape technologies. ADIC also offers specialized storage management software products as well as Fibre Channel Storage Area Network solutions with guaranteed interoperability and one-call support.

Alcatel
Booth 131
818-880-3500
john.lee@xylan.com
www.xylan.com

Alcatel, a $25 billion company, delivers integrated end-to-end voice and data network systems to enterprises, established and new carriers, and consumers worldwide. Alcatel's enterprise networks offer high performance, data security, and easy voice/data integration. Its service provider solutions offer high-speed Internet access products, advanced routing software, IP-VPN security, and comprehensive management.

Aironet
Booth 133
503-464-8396
mkatz@aironet.com
www.aironet.com

Alta Technology
Booth 857
801-562-1010
sales@altatech.com
www.altatech.com

Alta Technology, a long-time leader in high performance parallel and distributed systems, will display three families of Linux-based multiprocessor systems. Alta systems implement Alpha and Pentium processors,

high-speed interconnectivity such as SCI Myrinet or Gigabit Ethernet, and large-capacity storage options. On display will be the AltaCluster, the M-Cluster and the R-Cluster models. Various applications and demonstrations will also be shown.

Anthro Corporation
Booth 864
800-325-3841
sales@anthro.com
www.anthro.com

Take control of your space with AnthroCarts! Mobile, modular, incredibly strong furniture for all your personal computers, multimedia, and networking equipment. Lots of shapes, sizes, and accessories to choose from--configure them exactly the way you want for your set-up. AnthroCarts come with a lifetime warranty and ship within 24 hours! Call for a free catalog or order online.

Apple Computer, Inc.
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408-974-7406
simpson@apple.com
www.apple.com

Applied Metacomputing LLC
Booth 601
804-982-2204
grimshaw@appliedmeta.com
www.appliedmeta.com

Applied Metacomputing sells Legion and Legion-related services. Legion is a meta-operating system that allows very large collections of heterogeneous computers scattered across multiple organizations to be used and managed. Legion enables secure, cross-site, cross-platform program execution and resource sharing, yielding benefits of higher utilization, easier collaboration, and simpler application integration.

Aspen Systems, Inc.
Booth 951
303-431-4606
sales@aspsys.com
www.aspsys.com

Aspen Systems specializes in Alpha & Pentium Beowulf clustering solutions. Aspen's custom rackmount design incorporates up to 44 processors/rack using advanced networking technology, including Myrinet/LAN, Gigabit, and fibre. Integrated KVM switches, TFT screens, and customized software installations. Tru64 UNIX/Linux/NT OS. Aspen Systems also specializes in high-performance workstation and server solutions.

Association for Computing Machinery
Booth in lobby
800-342-6626; 212-626-0500
acmhelp@acm.org
www.acm.org

ACM, the Association for Computing Machinery, is an 80,000-member, international scientific and educational organization dedicated to advancing information technology. ACM publishes books, magazines (including the monthly magazine, Communications of the ACM), journals, and the ACM Digital Library

(200,000 searchable pages of journals and proceedings text from 1991 forward). ACM's Special Interest Group on Computer Architecture (SIGARCH) is a co-sponsor of the SC conference.

Cleanscape Software International
Booth 916
408-978-7000
monty@cleanscape.net
www.cleanscape.net/

Cleanscape Software develops a line of source code analyzers designed to improve the software development cycle. FORTRAN-lint and lint-PLUS analyze Fortran and C code, reporting problem areas that are not detectable by compilers. Cleanscape also markets an advanced software construction system called qef. qef is a complete replacement architecture for "make."
Highlight: Cleanscape Software will be demonstrating its advanced software construction system, qef. qef replaces "make" based systems with an architecture that is dedicated to the software construction process. It introduces high-level constructs that make simple, reliable, consistent, and portable software builds.
See also: Exhibitor forum

Compaq Computer Corporation
Booth 721
508-467-1499
kathleen.hudson@compaq.com
www.compaq.com

Compaq (NYSE: CPQ), the world's second largest computer company, provides a full range of computer systems, storage and network products, software, and services. Compaq's Alpha processor is the high performance market leader and the fastest microprocessor in the industry. Alpha systems deliver the best absolute performance, and the best price/performance available with Tru64 UNIX or Linux.
Highlight: At Compaq, our vision for maintaining this leadership is a tera-scale system using a high bandwidth, low latency, very scalable interconnect to link standard AlphaServer SMP platforms. Future microprocessor designs can also incorporate additional system infrastructure in silicon, further improving price/performance. These next-generation Alpha architectures will be highlighted in the booth.
See also: Exhibitor Forum

Computer Network Technology
Booth 819
612-797-6725
earl_schaefer@cnt.com
www.cnt.com

Computer Network Technology (CNT) provides hardware, software, and services for the implementation of storage-area networking and enterprise application integration solutions. Organizations worldwide choose CNT to build and run their business-critical networks and gain greater connectivity and access to information without sacrificing performance, security, or integrity.

Cray Research
Booth 681
651-683-7277
ellen@sgi.com
cray.com

Cray Research will feature presentations by leading U.S. and international customers; the Cray T3E, the

world's most powerful supercomputer and first to sustain a teraflop on a real-world application; the pioneering Cray SV1 scalable vector system; and talks on future product plans and other breakthrough developments for high-end supercomputer users.

CSP Inc. MultiComputer Division
Booth 432
978-663-7598
slcooper@cspi.com
www.cspi.com

The 2000 SERIES is a family of high performance multicomputer systems designed for use in a variety of compute-intensive applications, including radar, sonar, simulation, and surveillance signal processing. 2000 SERIES systems use Myrinet networking technology, Message Passing Interface (MPI) software for interprocessor communications, and the VxWorks real-time operating system.

Highlight: FOliage PENetration Synthetic Aperture Radar--FOPEN SAR: Target detection in dense foliage using CSPI's 2000 SERIES Systems. FOPEN SAR applications require very powerful Digital Signal Processing (DSP) systems with advanced networking technology for fast interprocessor communication. The demonstration will show the 2000 SERIES System from CSPI providing the high performance and superior networking technology to address this requirement.
See also: Exhibitor Forum

CS Systemes D'Information
Booth 848
331 53 68 3300
lionel.nouzarede@cssi.cie-signaux.fr
www.3ip.fr

CS Systemes d'Information, a multibillion-dollar worldwide informatics and telecommunication French company, is the European leader for scientific engineering. CS Systemes d'Information represents throughout Europe several HPC software vendors, including NAG, PGI, Etnus and Pallas, and is looking for new partners.

DataDirect Networks, Inc.
Booth 231
818-700-7600
jswenson@datadirectnet.com
datadirectnet.com

DataDirect Networks is the world's leader in the rapidly growing market for intelligent data-access SAN software infrastructures that address the most demanding requirements of high performance, cross-platform shared data access and integrated data management services. The company pioneered the concept of "shared network data access."

DCG Computers, Inc.
Booth 342
603-421-1800 x10
sjg@dcginc.com
www.dcginc.com

Dell Computer Corporation

Booth 866
512-728-6346
george_funk@dell.com
www.dell.com

Ranked No. 78 among the Fortune 500 companies and No. 210 in the Fortune Global 500, Dell Computer Corporation is the world's leading direct computer systems company, based on revenues of $21.7 billion for the past four quarters. Dell designs, manufactures, and customizes products and services to customer requirements and offers an extensive selection of software and peripherals.

Enron Communications, Inc.
Booth 912
503-464-8396
ted_seitz@enron.net
www.enron.net

Essential an ODS Networks Company
Booth 661
505-344-0080, ext.319
pheater@ods.com
www.esscom.com

Essential/ODS is the high performance division of ODS Networks. Essential's products are key building blocks for the world's fastest supercomputers and largest storage areas networks, and are used to deliver maximum speed and bandwidth to high performance workgroups. Our GSN and HIPPI networking products include switches and network interface cards.

Etnus, Inc.
Booth 847
651-994-4564
mkay@etnus.com
www.etnus.com

Etnus is a leading provider of software development tools for developers of complex, parallel and/or distributed applications in the High Performance Computing community. Etnus offers TotalView, a debugger that supports all major parallel programming models and TimeScan, an event-based performance analyzer. TotalView is the debugger of choice for the DOE ASCI program.
Highlight: Etnus will demonstrate its TotalView debugger running on AIX, IRIX, Tru64 Unix, and Linux platforms. TotalView is a multiplatform source-level graphical debugger for C, C++ and Fortran that supports multi-process and multi-threaded applications and parallel programming paradigms including MPI, PVM, and OpenMP.

FORE Systems, Inc.
Booth 402
742-742-4444
info@fore.com
www.fore.com

FORE Systems, a wholly owned subsidiary of The General Electric Company, p.l.c. (U.K.), is a leading global supplier of high performance networking solutions. FORE's Networks of Steel deliver the increased capacity, resiliency, and scalability necessary to build networks that last. Thousands of enterprise and service provider customers worldwide have put FORE Systems solutions at the heart of their networks.

Foundry Networks, Inc.
Booth 834
408.731.3800
info@foundrynet.com
www.foundrynetworks.com

See Foundry Networks' award-winning Layer 2-3 and Layer 4-7 Gigabit Ethernet products, like our BigIron chassis-based switching router that provides high-density Gigabit Ethernet and up to 96,000,000 pps performance. And our ServerIron Switch that includes an extensive suite of load balancing and transparent cache switching features. Experience IronClad Network Performance!

Fujitsu
Booth 741
713-267-2350
ronm@fujitsu.com
www.fujitsu.com

Visit the Fujitsu booth to experience the ultra-high-speed and power of the VPP5000 Series high-performance computers, the fastest supercomputers available today. The VPP5000 boasts record vector performance of 9.6 GFlops per PE and 4.9 TFlops for a 512-PE system, and features Fujitsu's concept of Fast, Flexible and Friendly high-performance computing.
Highlight: See demos of the VPP5000 Series, exhibiting how fast (fast performance, large memory, ultra-high-speed and flexible I/O), flexible (scalable from 1 to 512 PEs, flexible system administration), and friendly (UNIX operating system, browser-based system administration, compatibility with VPPx00 Series supercomputers preserves software assets, conforms to and supports industry standards) they are.
See also: Exhibitor Forum

GENIAS Software Inc.
Booth 817
410 455-5580
geniasna@istar.ca
www.geniasoft.com

CODINE manages the workload for fastest computer run times in heterogeneous clusters. GRD is a CODINE superset that manages the overall computing resources, including policies. It provides a single-system image (virtual mainframe) to users and systems administrators.

GENROCO
Booth 771
262-644-8700
sales@genroco.com
www.genroco.com/

GENROCO is displaying heterogeneous, high-speed network products including Gigabit Ethernet, GSN, HIPPI, and ATM bridges to Fibre Channel storage arrays utilizing the GENROCO TURBOstor bridge, the GENROCO 8-port GSN switch providing full duplex 6400 megabit (800 megabyte) per second data rates, and ST-enabled network interfaces for Compaq, SUN, SGI, and IBM.

GST Telecommunications, Inc.
Booth 922
360-356-2847
benpeek@gstis.net

www.gstcorp.com

GST Telecommunications, Inc. (NASDAQ: GSTX), a facilities-based Integrated Communications Provider (ICP) headquartered in Vancouver, Washington, provides a broad range of integrated telecommunications products and services. Offerings include enhanced data and Internet services and comprehensive voice services throughout the United States, with a robust presence in California and the West.
Highlight: GST Telecom and Nortel Networks present the National Transparent Optical Network (NTON) and the SC99 Experimental Network (Xnet). NTON, a DARPA-sponsored "SuperNet" project, is a next-generation OC192 network from San Diego to Seattle. Segments of NTON will connect research home sites to booths at SC99. Xnet is providing DWDM connections at SC99.

Hard Data, Ltd.
Booth 824
780-456-1510
maurice@harddata.com
www.harddata.com

Hard Data, Ltd. of Canada and HIT Corporation of Japan are jointly showing new technologies in Beowulf clusters based on the Alpha Processor Inc. 21264 Alpha CPU, AMD Athlon, and Intel solutions. Selected high performance workstation and server technologies, reflecting design goals of extreme performance and fault tolerance. Rack-mount and freestanding equipment, chassis, and related components for the serious HPC user.

Hewlett-Packard Company
Booth 201
905-206-3108
dmcdonnell@hp.com
www.hp.com/go/technical

HP manufactures technical servers and workstations that provide government, research, and commercial organizations with the best performance and reliability available. HP's PA-RISC architecture also offers the best investment protection path for moving forward. With its recent N-Class server, HP has redefined midrange technical servers with outstanding performance at midrange prices.
See also: Exhibitor Forum

Hitachi, Ltd.
Booth 221
81 463-88-8263
khayashi@kanagawa.hitachi.co.jp
www.hitachi.co.jp

From 1982 Hitachi has developed the S-series of vector supercomputers and the SR-series of MPPs for the numerically intensive computing market. Hitachi's latest machine is a teraflops computer, the SR8000, with several innovative design concepts. The SR8000 has both the high performance of a vector machine and the high scalability of a parallel-type supercomputer.
Highlight: Hitachi is currently making advertising efforts for its September released new SR8000 model. This new model possesses the world's highest theoretical peak performance of 6 TFlops.
See also: Exhibitor Forum

HNF
Booth 946
505-238-4344

dru@genroco.com
www.hnf.org

HPCwire
Booth 431
858-625-0070
jennifer@tgc.com
www.tgc.com

HPCwire is the publication of record for scientific and commercial high performance computing. Delivered worldwide each Friday via the Internet, HPCwire is the most complete and for many the sole source of information about this rapidly evolving field. For CIOs, IS managers, and technical professionals in business, government, and academia, HPCwire offers complete coverage of the latest developments in HPC.

HPSS
Booth 513
925-422-9216
dwatson@llnl.gov
www.sdsc.edu/hpss/

Rapid growth in dataset size is causing serious imbalances in I/O and in storage system performance and functionality relative to application requirements and the capabilities of other system components. The High-Performance Storage System (HPSS) is a scalable, next-generation storage system addressing these imbalances for large-scale scientific and commercial computing environments.

Hyperchip, Inc.
Booth 956
450-923-8882
lhardcastle@hyperchip.com
www.Hyperchip.com

Hyperchip provides extreme performance network systems with LAN, SAN, and WAN interfaces to integrate a customer's Internet access and local, server, and storage area networks into a single, seamless system. Hyperchip's massively parallel semiconductor technology scales from terabits to petabits per second, eliminating forklift router upgrades for the foreseeable future.
Highlight: The Hyperchip demonstration will show a Hyperchip(tm)-based server cluster running an entertaining application and juggling multiple uncompressed video streams.
See also: Exhibitor Forum

IBM
Booth 421
914-642-5182
rcopelan@us.ibm.com
www.rs6000.ibm.com/solutions/supercomputing/index.html

IBM offers a full range of high performance computing products and solutions. The company's Scientific and Technical Computing Group is made up of three segments-Government/Higher Education, Petroleum, and Manufacturing. IBM Research runs the Advanced Computing and Technology Center and the new Deep Computing Institute.
Highlight

Entries are listed alphabetically by surname of presenter.

High Performance and High Scalability

Yoshiro Aihara
Hitachi, Ltd.

Abstract:

From 1982, Hitachi has developed a S-series of vector supercomputer and a SR-series of MPPs for the numerically intensive computing market. Hitachi's latest machine is a Teraflops computer, SR8000, announced in May 1998, with several innovative design concepts. Several tens of SR8000 systems have already been installed. The new supercomputer, SR8000, has both the high performance of a vector machine and the high scalability of a parallel type supercomputer. It is therefore possible to use

the SR8000 either as a vector computer or a parallel computer. This architecture allows a flexible system operation as well as smooth transition from either of these machine types. To achieve the high, sustained performance of vector processor, the SR8000 supports the Pseudo Vector Processing function within a microprocessor, and Co-Operative Microprocessor in single Address Space (COMPAS) within a node.

FORESYS - A Suite for Fortran Software Engineering

Walt Brainerd
Unicomp, Inc.

- Abstract:

FORESYS is a suite of tools that enable the automated analysis, restructuring, quality control, and conversion of engineering and scientific codes. FORESYS includes automated tools for the conversion of legacy Fortran software to modular and maintainable Fortran90/95. The presentation will include a live demonstration of the FORESYS suite and a discussion of conversion issues for large legacy Fortran applications.

Architecting a New World of HPC

Shahin Khan
Sun Microsystems, Inc.

- Abstract:

The last decade of the 20th Century has seen myriad of changes in supercomputing and the markets the industry supports. Customers are moving from proprietary to commodity-based hardware as the preferred architectures for building Tflop-class systems. Equally important is the change to the overall usage model. As the Web and Internet technologies become more widely deployed, the usage model continues to evolve. The Web is a key component to enabling collaborative computing and Sun has been an integral supplier and leader of this evolution. This revolution in the usage model will have a dramatic impact on all aspects of computing as we move to the next paradigm. Sun Microsystems, Inc. will cover future directions including technologies related to high performance networking and portal computing to enable truly collaborative supercomputing and the new applications that are being developed in order to further enable the Information Utility Era.

High Performance Servers and Interconnects: The Next-generation Supercomputers

Richard Kaufmann
Compaq Computer Corporation

- Abstract:

Market dynamics are critical in the design of next generation supercomputers. With programs like the Accelerated Strategic Computing Initiative (ASCI), the requirements of our most demanding customers have never been more clearly defined. However, the economic failure of specialized HPC

architectures strongly suggests that we find another approach to designing the supercomputers of the future, one that leverages high-volume, low-cost components wherever possible. At Compaq, our vision for meeting ASCI requirements is a tera-scale system using a high bandwidth, low latency, very scalable interconnect to link standard AlphaServer SMP platforms. This parallel server functions as a single, highly available system and delivers the highest absolute performance, as well as the best performance-cost ratio. Future microprocessor designs can also incorporate additional system infrastructure in silicon, further improving performance-cost characteristics. Finally, the scalability of the architecture-from one SMP no node to hundreds-allows it to serve commercial as well as technical customers.

Defect Tolerant Molecular Electronics

Philip J. Kuekes

Hewlett-Packard Laboratories

- Abstract:

  In order to build complex systems of ever-smaller components, we must find a new technology that will allow massively parallel construction of electronic circuits at the atomic scale. We are working on a defect tolerant reconfigurable architecture that allows one to electrically download the designed complexity of a computer into a chemically assembled imperfect nanostructure (Science, v.280, 12 June 1998). Our Hewlett-Packard and University of California research team is currently developing the molecular building blocks for this technology (Science, v.285, 16 July 1999.) The industrial revolution started with inexpensive labor assembling capital-intensive interchangeable precision parts. Two centuries later we may switch to supercomputer labor assembling inexpensive chemically produced imperfect parts.

Platform's LSF Suite and Intel-based Multiprocessing Workstations in Action

Brian MacDonald

Platform Computing Corp.

- Abstract:

  Platform Computing is an acknowledged global leader in application resource management-the effective management of computing workload to support business-critical applications and processes. Platform's LSF Suite transparently harnesses computing resources in distributed heterogeneous UNIX and Windows NT environments, enabling the workload to be handled faster to achieve increased productivity and processing efficiency.

The CDK Cluster Development Kit: Parallel Fortran, C and C++ compilers and Tools for Linux Clusters

Douglas Miles

The Portland Group, Inc.

- Abstract:

In combination with the Linux operating system, The Portland Group CDK enables use of networked clusters of Pentium II/III workstations and servers to tackle serious scientific computing applications. The PGF77 and PGF90 Fortran compilers and the PGCC C and C++ compilers include full native support for OpenMP shared-memory parallel programming for effective use of multi-CPU cluster nodes. The PGHPF High Performance Fortran compiler enables development of high-level distributed memory parallel programs. The Portland Group CDK also includes a custom installer and pre-configured versions of the most common open source cluster utilities: MPI, the PBS batch queuing system, the ScaLAPACK parallel math library, PVM, and example and tutorial programs. This presentation will provide an overview of The Portland Group CDK along with descriptions of applications and benchmark results obtained using The Portland Group CDK compilers and tools.

Deep Computing

Jamshed Mirza
IBM

- Abstract:

Scalable systems such as the IBM RS/6000 SP hold the promise of "unlimited" cost-effective performance that can truly unlock the promise of Deep Computing. This presentation will highlight the systems trends and Deep Computing applications dynamics over the next few years that will enable strategically important solutions in both commercial and technical areas.

Vector-Parallel Systems: Powerful High Performance Computers

Kenichi Miura
Fujitsu

- Abstract:

This presentation will talk about the features of the 64-bit architecture VPP5000 supercomputers, the latest generation of vector-parallel supercomputers from Fujitsu. It will cover the hardware and software features such as the new vector and scalar units, and the crossbar network, which provides ultrahigh-speed large-capacity processing. The performance of various commercially available software applications will also be discussed.

Network Systems that Scale to Petabit Levels

Richard Norman
Hyperchip, Inc.

- Abstract:

Hyperchip, Inc. is a Montreal company that is building network systems that scale to petabit levels. Hyperchip's products are based on massively parallel semiconductors, a revolutionary architecture that produces a tremendous increase in system performance while reducing complexity and costs. While traditional high-end architectures require numerous custom chip designs, each with a few extremely

complex functional units, Hyperchip's architecture builds a massively scalable system from a network of identical chips, each of which contains a repetitive array of hundreds of simple, efficient units. In addition to greatly reducing system size, cost, and power consumption and eliminating serial bottlenecks, Hyperchip's architecture reduces design costs by leveraging the massive replication of simple units. The tremendous advantages of massively parallel semiconductors can be applied to a wide variety of computing and communications components. Because the key challenge across today's server, storage, local- and wide-area networks is switching and routing scalability, Hyperchip has applied this technology to build routing systems that scale to tens of thousands of multi-gigabit ports.

Progress Toward a New Capability Architecture

Steve Oberlin
SGI

Abstract:

Supercomputing applications can be generally sorted and plotted onto a spectrum colored by communications and synchronization characteristics. At one extreme of the communications/synchronization spectrum, call it the "embarrassingly parallel" (EP) end, we plot codes that require little or no communications between cooperating compute nodes. At the other end of the spectrum, we plot "communications intensive" (CI) codes that require larger quantities of global communications perhaps exacerbated by fine granularity or irregular patterns. Any parallel architecture runs codes that are closer to the EP end of the communications/synchronization spectrum better than those at the CI end do. Since often-reasonable performance on EP codes is all that is required to solve a problem, acceptable performance is generally available in a number of inexpensive clustered/COTS systems. However, many interesting and important problems can only be solved by algorithms with strong CI characteristics that unfortunately perform quite poorly on clustered/COTS systems, making designed-for-CI architectures a critical class of supercomputers.

Parallel and Distributed Computing for the Biotech and Financial Industries

Andrew Sherman
Scientific Computing Associates, Inc.

Please report comments to sc99proceedings@sc99.org
Last Modified: Sep 25 1999

Abstract:

High performance parallel and distributed computing is of growing importance in many industries, but especially in biotechnology and finance. Scientific Computing Associates, Inc. is partnering with leading hardware and software vendors to help these industries leverage cutting-edge developments in both parallel algorithms and computational infrastructure (processors, networks, operating systems, and languages). This presentation describes several of Scientific's recent initiatives, including: JParadise(r) and JPiranha(r), tools based on Java for distributed computing on the Internet; Linda(r) and Paradise(r) for Linux on Intel and Alpha systems; Linda for clusters of SMPs and the VI communication architecture; and parallel applications for molecular modeling, image analysis, and risk management. Scientific is a leading commercial developer of parallel and distributed software tools, middleware, and applications. Products from Gaussian (the ab initio quantum chemistry program) to Crystal Ball Turbo (an Excel-based parallel Monte Carlo simulation tool) depend on Scientific's technology.

SC·99

Portland and Oregon
Travel & Tourism Information

You're probably from the Northwest if you ...

General Information about Portland

Portland, Oregon often appears in Marjabelle Young-Stewart's top five (and always in the top ten) listing of "Most Polite Cities in America." Travel & Leisure magazine in a headline even declared: "Portland: Everything you always wanted in a city but were afraid to ask for." Other notables about the 27th largest metro area in the country include:

- Among the Ten Best Managed Cities, Financial World magazine
- Among the Top Ten American Walking Cities, Walking magazine
- One of the America's Top 20 Best Places to Work, Employment Review
- One of Four Cities Most Likely to Weather a Recession, U.S. News and World Report
- 16th Best Place to Live out of 351 Metro Markets, Places Rated Almanac

The SC conference is returning to Portland in 1999 due to the city-wide support and success of SC93. Attendees will find world-class dining and performing arts, snow-capped mountains, recreational activities in thousands of acres of parks, sidewalks paved with famous quotes, a bevy of brews served up by local microbreweries and specialty coffee shops, and the largest bookstore in the United States. Portland's arts and entertainment range from chamber music concerts to clubs featuring jazz, blues, and alternative rock 'n' roll, making Portland live up to its newest nickname, "Hip City." Also known as the "City of Roses," Portland is home to the International Rose Test Garden, where more than 500 varieties of roses bloom.

Attractions

Notable attractions include the Oregon Zoo, the Oregon Museum of Science and Industry, the Japanese Gardens, the International Rose Test Garden, and the Portland Art Museum.

Arts and Entertainment

Portland's performing arts include a proud tradition of live theatre productions, creative dance, and musical presentations. In addition, spectator sports include Arena Football, Baseball, Basketball, Hockey, Racing (Auto, Horse, and Greyhound), and Soccer.

Other Amenities

Portland's shopping includes upscale outlets, unique shops, restaurants, coffeehouses, and large malls. No sales tax means many out-of-state visitors can be found here.

Outdoor activities include skiing, golf, running, tennis, windsurfing, fishing and hunting. There are also 223 state parks and campgrounds, 50 of which allow overnight camping, which are located within the state's most spectacular scenic regions.

Half-day tours include trips to the Columbia Gorge National Scenic Area and Mt. St. Helens (allow 4 to 8 hours).

Additional Information

Additional details about what Portland has to offer can be found at:

- www.pova.com
- travelportland.com
- www.katu.citysearch.com
- www.traveloregon.com
- Any of the links which appear below!

or by calling the Portland Oregon Visitors Association at 1-87-PORTLAND.

Links to additional Portland/Oregon information are offered below.

Oregon Convention Center

- Oregon Convention Center
- Area Restaurants
- Map of area hotels, attractions and shopping

Portland Area Info

- Portland Oregon Visitors Association
- City Search guide to Portland
- Sidewalk Portland
- Portland Maps
- Portland Weather
- The Oregonian Diner
- Microbrewery Guide

Recreation and Entertainment

- The Oregonian's Oregon Live
- Oregon Symphony
- Portland Online MusicNet
- Farmers' Markets in Portland
- Portland Saturday Market
- Portland Metro Golf Guide

- Bus tours around Portland
- Oregon Museum of Science and Industry
- Oregon Historical Society Museum
- Portland Art Museum
- Oregon Maritime Center and Museum
- World Forestry Center
- International Rose Test Garden
- Portland Zoo
- Portland Parks and Recreation

Other Places within Easy Travel Distance

- Columbia River Gorge National Scenic Area
- Scenic Driving in the Columbia Gorge area
- Columbia Gorge Discovery Center
- Hiking in the Columbia Gorge area
- Hiking (statewide)
- Timberline Lodge(ski area and historic hotel on top of Mt. Hood)
- Windsurfing in the ColumbiaGorge area
- Cross-country and downhill skiing (67 miles from Portland)
- Oregon Tourism Commission
- Great Outdoor Recreation Guide
- Gilbert's Discovery Village and Toy Hall of Fame (museum of Erector Set's creator - in Salem)
- Maryhill Museum of Art(Columbia Gorge area)
- Oregon Electric Railway Museum (between Portland and Salem)
- Oregon Brewers Guild - Microbrewery guide
- Oregon Wineries Guide

Professional Sports Teams

- Portland Trailblazers (Basketball)
- Portland Winterhawks (Hockey)
- Portland Python (Soccer)
- Portland Pride (Basketball - ABL)
- Portland Forest Dragons (Arena Football)

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SC99

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November 13-18, 1999

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