2015 ACM/EDAC/IEEE
DESIGN AUTOMATION CONFERENCE
(DAC)

June 7-11, 2015
Moscone Center
San Francisco, CA. United States

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GENERAL CHAIR'S MESSAGE

Dear Colleagues,

Welcome to the 52nd Design Automation Conference, once again in San Francisco: the cultural, commercial and financial center of Northern California. And for this week, San Francisco is the design automation capital of the world!

Led by the DAC executive committee, countless volunteers who help pull together the conference have excelled once again, bringing you a program filled with incredible research and industry presentations. Our 175+ vendors, an integral part of the conference ecosystem and great contributors to our success, will showcase recent technology advances in design automation, foundry solutions, embedded systems and software, and IP.

DAC is unique in bringing together industry and university researchers, designers, developers, vendors and training partners. There is no better conference for learning and networking, activities which of course aren't limited to the technical sessions. Join us for networking every day at 6:00pm: Monday and Tuesday for the first time on the show floor, and Wednesday on the Moscone Esplanade.

Our industry is doing well and achieved record revenue last year, according to an April 2014 EDAC report. It has also been a year of good news for DAC. We received record submissions for a slew of conference areas, including the research, designer and IP tracks, as well as for tutorials and collocated events. We're continuing our investment in embedded systems and software content, which as in recent years will make up a third of the program. We had more than 1,000 "I love DAC" registrations in the first week alone and more than 30,000 views of our weekly blog over the last nine months.

Here are some forthcoming #DAC52 highlights by the numbers:

- 4 amazing Keynote Sessions and 1 Visionary Moore's Law Talk
- 8 interesting SKY (short keynote) Talks
- 9 Tutorials, 9 Workshops, and 6 Colocated Conferences
- 2 Management Day Sessions
- 24 Special Sessions and Panels
- 27 Research Paper Sessions
- 21 Designer and IP Track Sessions, and a special poster networking session on Tuesday at 4:30pm.
- 6 training sessions on Thursday by Doulos

Make sure to check out the DAC pavilion program and make your way there for the twice daily SKY talks—we moved them to the exhibit floor to make it easier to attend and are featuring some very interesting speakers you don't want to miss.

With our mobile app we are making DAC more fun this year with a game called DAC Attack. You can find details online or just ask ask anyone with an official DAC shirt how to play and compete for several cool prizes including an Apple Watch.

Enjoy the #52DAC!

Anne Cirkel
General Chair, 52nd DAC

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Politecnico di Torino
Torino, Italy

Haibo Zeng
Virginia Polytechnic Institute and State Univ.
Blacksburg, VA

PANEL CONTRIBUTORS

Graham Bell
Real Intent
Sunnyvale, CA

Gene Forte
Mentor Graphics Corp.
Wilsonville, OR

Valeria Bertacco
Univ. of Michigan
Ann Arbor, MI

Anne Cirkel
Mentor Graphics Corp.
Wilsonville, OR

Saverio Fazzari
Booz Allen Hamilton, Inc.
Clarksville, MD

Harry Foster
Mentor Graphics Corp.
Wilsonville, OR

Ramesh Karri
New York Univ.
Brooklyn, NY

Andrew B. Kahng
Univ. of California at San Diego
La Jolla, CA

Hai Li
Univ. of Pittsburgh
Pittsburgh, PA

Debajani Majhi
Broadcom Corp.
San Diego, CA

Mac McNamara
Adapt-IP
Paolo Alto, CA

Natesan Venkateswaran
IBM Corp.
Hopewell Junction, NY

MONDAY KEYNOTE ADDRESS
June 8, 2015
Gateway Ballroom 9:20am

Google Smart Lens: IC Design and Beyond

Brian Otis - *Google, Inc., Mountain View, CA*

Abstract: We have amazingly sparse access to information about our own bodies. Indeed, the healthier we are, the less data we collect. Technologies to continually monitor critical biomarkers are still in their infancy, but continuing advances in chip design and biocompatible system integration will help define the next generation of these devices. Against the backdrop of the Google Smart Contact Lens platform, I'll share thoughts on the scarcity of power, extreme miniaturization, and end-to-end connected systems that span the design space from transistors to the cloud. Along the way, I'll cover chip design techniques for body-worn systems and wireless sensors and present examples of constantly-connected devices for improving healthcare. These areas present tough unsolved problems at the interface between the IC and the outside world that cannot be solved by transistor Tech. scaling alone. The interface between silicon and the human body is highly variable, erratic, and messy. This unpredictability impacts sensor performance, RF/electromagnetic performance, system reliability, tolerability and comfort, etc. Several future applications will demand thin-film realization and biocompatibility of complex systems. Novel power sources, low power IC design techniques, microscale user interface technologies, and new system integration techniques will be a few of the enabling technologies for these emerging systems.

Biography: Dr. Brian Otis is a Director at Google [x] and a Research Associate Professor at the Univ. of Washington, Seattle. He received a B.S. in electrical engineering from the Univ. of Washington, Seattle, and a M.S. and Ph.D. degree in electrical engineering from the Univ. of California, Berkeley. He joined the faculty of the Univ. of Washington in 2005 where he founded a chip design research lab that develops tiny, low power wireless chips for a variety of applications (neural recording, implantable devices, wearable on-body wireless sensors, environmental monitoring, etc). He has previously held positions at Intel Corp. and Agilent Technologies and has been with Google Inc since 2012. He is a founder of Google [x]'s smart contact lens project and leads the Microsystems group at Google Life Sciences. He has served as a member of the Technical Program Committee of the International Solid-State Circuits Conference (ISSCC) and Associate Editor of the Journal of Solid State Circuits (JSSC). His research interests include low power SoC design, exploring limitations of power and size of wireless systems, and the realization of novel biomedical devices.

TUESDAY VISIONARY TALK ADDRESS
June 9, 2015
Gateway Ballroom 9:00am

Moore's Law at Fifty: No End in Sight

Vivek Singh – *Intel Corp., Hillsboro, OR*

Abstract: Moore's Law is an observation that a transistor – the fundamental building block of the digital age – will decrease in cost at a steady, exponential rate. This decrease in cost as well as transistor size over the past 50 years has also led to dramatic increases in compute power and energy efficiency and transformed our world with ever-more powerful smart phones, tablets, personal computers and data centers. It has also enabled computing to become a powerful yet invisible force in our homes, offices, cars, factories and much more. These imperatives are the reason Moore's Law will continue, and motivated teams will continue to find innovative solutions to the engineering challenges of the day, just as they have in the past. This talk will provide some examples of how complex problems have been overcome in recent technology nodes, including those from the field of Computational Lithography. Inverse Lithography and Source Mask Optimization are two such examples that have helped extend the life of 193 patterning. Such innovations, fed by a rich technology pipeline, give us confidence that Moore's Law will continue.

Biography: Vivek Singh is an Intel Fellow and director of computational lithography in Intel's Technology and Manufacturing Group.

He is responsible for all of Intel's CAD and modeling tool development in full chip OPC, lithography verification, rigorous lithography modeling, next-generation lithography selection, inverse lithography technologies and double patterning. He also represents Intel on several external Design for Manufacturability (DFM) forums, and is currently President of the Lithography Workshop. He holds over 20 patents, has published over 50 technical papers and he and his team have won Four Intel Achievement Awards.

Singh graduated from the Indian Institute of Technology in Delhi with a bachelor's degree in chemical engineering in 1989. He earned a master's degree in chemical engineering in 1990, a Ph.D. minor in electrical engineering in 1993, and a Ph.D. in chemical engineering in 1993, all from Stanford University.

TUESDAY KEYNOTE ADDRESS
June 9, 2015
Gateway Ballroom 9:15am

The Design of Innovation That Drives Tomorrow

Jeffrey Owens – *Delphi Automotive, Troy, MI*

Abstract: When people think of high tech devices, they rarely think of their cars, trucks or vans. Similar to the computational power of the human brain, today's vehicles possess more processing power than anything most consumers own or will purchase. A typical car is equipped with more than 50 computers designed to operate at automotive grade capabilities for an extended period of time. Vehicle manufacturers and automotive suppliers around the world are responding to a myriad of consumer preferences and regulatory initiatives -- including enhanced safety features, increased fuel economy, reduced emissions and connectivity. Vehicles of the future will require increased amounts of embedded software and electrical/electronic systems. Addressing this dynamic will require significant design automation aids to handle extreme complexity. Electronics and design automation will play a critical role in shaping the future of automotive by providing design Tech. that helps save lives, protect the environment and provide a satisfying in-car experience for drivers and passengers alike.

Biography: Jeffrey J. Owens is chief Tech. officer and executive vice president of Delphi Automotive, a $17B global automotive systems supplier. Owens is responsible for the enterprise information Tech. function and Delphi's global engineering organization, which includes more than 19,000 technologists located in 15 major technical centers. Owens leads the company's innovation strategies while driving advanced technologies supporting the global megatrends of safe, green and connected. Owens has served in a variety of engineering, manufacturing, finance and product line assignments. He served as president of Delphi Asia Pacific from 2006 to 2009. In his most recent assignment, Owens served as president of Delphi's Electronics & Safety division, establishing key growth product lines including active safety, power electronics for EV/HEVs and consumer connectivity electronics. Owens earned a bachelor's degree in engineering from Kettering Univ. and a master's degree in business from Ball State Univ. He currently serves as chairman of the Kettering Univ. Board of Trustees.

WEDNESDAY KEYNOTE PANEL
June 10, 2015
Gateway Ballroom 9:00am

Cyber Threats to Connected Cars: Staying Safe Requires More Than Following the Rules of the Road

Jeffrey Massimilla – *General Motors Company, Warren, MI*
Craig Smith – *Theia Labs / OpenGarages.org / IATC, Seattle, WA*

Abstract: Mobile computing has emerged as the largest Tech. platform ever deployed in human history. It is transforming our society, our economy and our everyday life in unforeseen and unprecedented ways. Combination of ever improving computing power driven by Moore's law and seamless wireless communication is enabling an array of innovative products and services. Trend towards ubiquitous computing is accelerating, where countless small embedded processors are connected wirelessly to the cloud. Moving toward next decade, mobile computing with increased reliability and wireless capacity in concert with internet of everything and cloud computing will sustain the industrial growth. Mobile devices drive a natural trend toward Tech. integration to achieve desired form factor, cost, battery life and performance. Key Tech. drivers include energy management, heterogeneous computing, novel brain inspired computer architectures, semiconductor process Tech. innovations, monolithic 3D integration, advanced thermal mitigation, new memory Tech. and smart RF. Advent of reliable, scalable and secure wireless Tech. will be crucial in sustaining the mobile computing market growth. In this talk, we will review the state of the art in mobile computing and related key Tech. drivers.

Biography: Jeffrey Massimilla was named chief product cybersecurity officer, Vehicle and Vehicle Services Cybersecurity for General Motors Company effective September 2nd, 2014. This role, was expanded from Massimilla's most recent position as director, vehicle cybersecurity.

Massimilla is responsible for leading the team that is developing and implementing protocols and strategies to reduce the risks associated with cybersecurity threats related to the vehicle and vehicle connected services. Prior to this role, he served as the engineering manager, Next-Generation Infotainment Systems and Integrations. During his time in this role, Massimilla led the development and launch of a fully new vehicle infotainment system. Joining GM in 2001, as a design release engineer, Massimilla held multiple roles both in electrical and vehicle product program engineering creating solutions for various in-vehicle components. Jeff holds a Bachelor's Degree in Electrical Engineering from the Univ. of Michigan and Master's degrees in Industrial and Manufacturing Engineering and Business Administration from the Univ. of Michigan.

Biography: Craig Smith is the founder of OpenGarages.org, a community driven vehicle research and exploration group. Craig also runs a security consulting firm, Theia Labs, which specializes in reverse engineering and automotive security. Craig has participated as a mentor for several automotive hack-a-thons with Battelle, US Cyber Camp and H3. He also published the 2014 Car Hacker's Manual which is available for free under the Creative Commons license. Craig has produced several open source tools and utilities to accelerate learning and research. Some of these tools include a web based group CAN bus sniffing tool, a tool to fingerprint active BUS network to determine make and model of a vehicle passively without causing network traffic, as well as some penetration testing tools targeted to vehicle communications.

Craig Smith currently works closely with automotive manufactures, after market specialists, government organizations and public awareness groups like I am the Calvary (IATC). Craig focuses on collaboration efforts between independent researchers and industry groups entering the array of internet connected equipment. He recently moved to Seattle and started an Open Garage there at Crash Industries.

Moderator Biography: John McElroy is the host of "Autoline Daily" the first industry webcast of industry news and analysis. He is also the host of the television program "Autoline This Week," an Emmy Award-winning, weekly half-hour discussion program featuring top automotive executives and journalists. McElroy also hosts "Autoline After Hours," the first regularly scheduled live webcast about the industry. The shows can be seen online at www.autoline.tv McElroy also broadcasts daily segments on WWJ Newsradio 950, the CBS affiliate in Detroit. He writes a monthly op-ed article for Ward's Auto World.

THURSDAY KEYNOTE ADDRESS
June 11, 2015
Gateway Ballroom 9:15am

Electronics for the Human Body

John Rogers – *Univ. of Illinois at Urbana-Champaign*

Abstract: Biology is soft, curvilinear and adaptable; silicon Tech. is rigid, planar and immutable. Electronic systems that eliminate this profound mismatch in properties create opportunities for devices that can intimately integrate with the body, for diagnostic, therapeutic or surgical function with important, unique capabilities in biomedical research and clinical healthcare. Over the last decade a convergence of new concepts in materials science, mechanical engineering, manufacturing techniques and device designs has led to the emergence of diverse classes of 'biocompatible' electronics. This talk describes the key ideas, with examples ranging from 'cellular-scale' light emitting diodes that can be injected into the brain for optogenetic behavioral control to bioresorbable electronics that can serve as non-antibiotic bacteriocides for treating surgical site infections.

Biography: Professor John A. Rogers obtained BA and BS degrees in chemistry and in physics from the Univ. of Texas, Austin, in 1989. From MIT, he received SM degrees in physics and in chemistry in 1992 and the PhD degree in physical chemistry in 1995. From 1995 to 1997, Rogers was a Junior Fellow in the Harvard Univ. Society of Fellows. He joined Bell Laboratories as a Member of Technical Staff in the Condensed Matter Physics Research Department in 1997, and served as Director of this department from the end of 2000 to 2002. He is currently Swanlund Chair Professor at Univ. of Illinois at Urbana/Champaign, with a primary appointment in the Department of Materials Science and Engineering, and joint appointments in several other departments, including Chemistry. He is Director of the Seitz Materials Research Laboratory. Rogers' research includes fundamental and applied aspects of materials for unusual electronic and photonic devices, with an emphasis on bio-integrated and bio-inspired systems. He is a member of the National Academy of Engineering and the American Academy of Arts and Sciences. He won a MacArthur Fellowship in 2009, the Lemelson-MIT Prize in 2011 and the Smithsonian Award for Ingenuity in the Physical Sciences in 2013.

TECHNICAL PANEL ABSTRACTS

SESSION 18: Design for Hardware Security: Can You Make Cents of It?
TUESDAY June 09, 1:30pm - 3:00pm | Room 300
TRACK: SECURITY | TOPIC AREA: SECURITY

Moderator: Saverio Fazzari - *Defense Advanced Research Projects Agency, Washington, DC*
Organizer: Saverio Fazzari - *Defense Advanced Research Projects Agency, Washington, DC*

Given the proliferation of counterfeit electronics in the supply chain, recent breaches at major retailers and the ever-growing Internet of Things, there is evidence that electronic hardware is the "new frontier" for security compromise. Yet the protection of hardware continues to take a back seat to software in cyber-defense. How real is the problem of hardware security? Should there be a stronger push to develop and deploy security techniques in design? Finally, is there money to be made in hardware security? Who benefits and who pays?

Panelists:
Ingrid Verbauwhede - *Katholieke Univ. Leuven, Belgium*
Siva G. Narendra - *Tyfone, Inc., OR*
Vincent Zimmer - *Intel Corp., Seattle, WA*
Dino A. DaiZovi - *New York Univ., New York, NY*
Lisa McIlrath - *Raytheon BBN Technologies, Cambridge, MA*

SESSION 28: Does DFM Now Stand for "Don't Forget About Me"?
TUESDAY June 09, 4:30pm - 6:00pm | Room 304
TRACK: EDA | TOPIC AREA: DESIGN FOR MANUFACTURABILITY

Moderator: Andrew B. Kahng - *Univ. of California at San Diego, San Diego, CA*
Organizer: Andrew B. Kahng - *Univ. of California at San Diego, San Diego, CA*

At 20nm and below, manufacturing techniques have led to a regime of extreme rule-based IC design. Design for manufacturability has been replaced by "design-Tech. co-optimization": ground rules from foundries, libraries from IP providers, place-and-route tools from EDA vendors. But, while designers might now have freedom-from-choice, today's reality is one of long design cycles, with poor incremental value at leading-edge nodes. Why is this happening? How much of the value proposition of a new Tech. is lost in making it accessible to designers? Who is responsible for losing this value?

Panelists:
Mahbub Rashed - *GLOBALFOUNDRIES, Cupertino, CA*
Kee Sup Kim - *Synopsys, Inc., Mountain View , CA*
Karim Arabi - *Qualcomm Technologies, Inc., San Diego, CA*
Julien Ryckaert - *IMEC, Leuven, Belgium*
Vivek Singh - *Intel Corp., Hillsboro, OR*

SESSION 40: Are You Ready for the Rigors of Automotive Reliability?
WEDNESDAY June 10, 1:30pm - 3:00pm | Room 303
TRACK: AUTOMOTIVE | TOPIC AREA: AUTOMOTIVE SYSTEMS

Moderator: Matthew Hogan - *Mentor Graphics Corp., Wilsonville, OR*
Organizer: Gene Forte - *Mentor Graphics Corp., Wilsonville, OR*

The electronics design community is looking to the automotive market with new eyes as the digital content of modern vehicles is skyrocketing. While everyone would like a piece of the pie, are potential new market entrants really prepared for the rigors of automotive electronics reliability? Is it possible to adapt existing designs to meet the reliability requirements of automotive systems? What about in-vehicle infotainment systems: from a reliability standpoint, are they just like consumer products, or do they have their own special requirements? What technical, process and cultural changes are needed to be successful in transportation industries?

Panelists:
Ofer Tamir - *TowerJazz, Netanya, Israel*
Ertugrul Demircan - *Freescale Semiconductor, Inc., Eugene, OR*
Ron Miller - *Delphi Automotive, Kokomo, IN*
Ray Notarantonio - *Infineon Technologies Americas, Livonia, MI*

SESSION 48: Scalable Verification: Evolution or Revolution?
WEDNESDAY June 10, 4:30pm - 6:00pm | Room 304
TRACK: EMBEDDED SYSTEMS
TOPIC AREA: TEST AND VERIFICATION

Moderator: Brian Baily – *Semiconductor Engineering, Beaverton, OR*
Organizers: Graham Bell – *Real Intent, INc., Sunnyvale, CA*
Harry Foster - *Mentor Graphics Corp., Plano, TX*

The EDA industry has made great strides in improving IP blocks and subsystem designs through the adoption of industry verification standards, such as SystemVerilog, Unified Power Format (UPF), Unified Coverage Interoperability Standard (UCIS), and the Universal Verification Methodology (UVM). While the industry generally agrees on methodologies used to verify IP blocks or subsystems, we lack consensus on approaches required to verify SoC integration and system-level functionality of embedded systems. Can existing standards and methodologies be extended to address system-level challenges, or are new approaches required?

Panelists:
Hillel Miller - *Freescale Semiconductor, Inc., Austin, TX*
Mark Glasser - *NVIDIA Corp., Santa Clara, CA*
Ali Habibi - *Qualcomm, Inc., San Diego, CA*
Steven Jorgensen - *Hewlett-Packard Co., Sacramento, CA*
Bill Greene - *ARM Ltd., Austin, TX*

SESSION 71: The Long and Winding Road to IoT Connectivity: Are We There Yet?
THURSDAY June 11, 4:00pm - 5:30pm | Room 304
TRACK: EDA
TOPIC AREA: GENERAL INTEREST

Moderator: Nick Sargologos - *Freescale Semiconductor, Inc., Austin, TX*

The anticipated vast growth of IoT devices and applications will be demanding for current network operators: this large scale deployment of potentially inefficient, insecure and even defective IoT devices can lead to critical challenges that impair connectivity for all users, or even worse, bring the network down completely. The way forward is like a winding road: What is the best IoT connectivity solution to address the key challenges of signaling, security, presence detection, power consumption and bandwidth? Will WiFi or low-power radio interfaces suffice, or will we need something new?

Panelists:
Aveek Sarkar - *ANSYS, Inc., San Jose, CA*
Alex Jinsung Choi - *SK Telecom Co., Ltd., Seoul, Republic of Korea*
Oleg Logvinov - *IEEE & STMicroelectronics, New York, NY*
Chris Rowen - *Cadence Design Systems, Inc., San Jose, CA*
Dave Flynn - *ARM Ltd., Cambridge, United Kingdom*

AWARDS

Marie R. Pistilli Women in EDA Achievement Award

For her significant contributions in helping women advance in the field of EDA Tech.
Margaret Martonosi, *Princeton Univ.*

P.O. Pistilli Undergraduate Scholarships for Advancement in Computer Science and Electrical Engineering

The objective of the P.O. Pistilli Scholarship program is to increase the pool of professionals in Electrical Engineering, Computer Engineering, and Computer Science from under-represented groups (women, African-American, Hispanic, Native American, and physically challenged). In 1989, ACM Special Interest Group on Design Automation (SIGDA) began providing the program. Beginning in 1993, the Design Automation Conference provided the funds for the scholarship and a volunteer committee continues to administer the program for DAC. DAC normally funds a $4000 scholarship, renewable up to five years, to graduating high school seniors.

The 2015 Recipients are:

Antonio Anguliar
Attending: California Polytechnic State Univ. in San Luis Obispo

Moie Uesugi
Attending: Brown Univ.

EDAC – IEEE/CEDA Phil Kaufman Award Re-Presentation

Honoring an individual who has had demonstrable impact on the field of electronic design through contributions in Electronic Design Automation (EDA).

Dr. Lucio Lanza, Lanza Tech Ventures, for providing innovative EDA and IP companies with exceptional vision, mentoring, and financial support.

IEEE CEDA Outstanding Service Award

For outstanding service to the EDA community as DAC General Chair in 2014.
Soha Hassoun, *Tufts Univ.*

IEEE CEDA Outstanding Service Award

For outstanding service to the EDA community as ICCAD General Chair in 2013.
Jörg Henkel, *Karlsruhe Institute of Tech. (KIT)*

IEEE Fellow

For contributions to hardware/software codesign of embedded computing systems.
Jörg Henkel, *Karlsruhe Institute of Tech. (KIT)*

IEEE Fellow

For contributions to mixed-Tech. micro-systems education.
Steven P. Levitan, *Univ. of Pittsburgh*

IEEE Fellow

For contributions to VLSI design for manufacturability.
Michael Orshansky, *Univ. of Texas at Austin*

IEEE Fellow

For contributions to design automation and architecture of three-dimensional integrated circuits.
Yuan Xie, *Univ. of California at Santa Barbara*

IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems Donald O. Pederson Best Paper Award

Kai Hu, Feiqiao Yu, Tsung-Yi Ho, Krishnendu Chakrabarty, "Testing of Flow-Based Microfluidic Biochips: Fault Modeling, Test Generation, and Experimental Demonstration,"
Vol. 33, Issue 10, pp. 1463 - 1475, October 2014.

A. Richard Newton Technical Impact Award in Electronic Design Automation

Sponsored by the IEEE Council on EDA and the ACM Special Interest Group on Design Automation
For pioneering contributions in the discovery and use of silicon physical unclonable functions (PUFs) for the design and operation of secure integrated circuits and systems.

Blaise Gassend, Dwaine Clarke, Marten van Dijk, and Srinivas Devadas, "Silicon Physical Random Functions," Proc. of the 9th ACM Conference on Computer and Communications Security, pp 148 – 160, November 2002

Blaise Gassend, Google
Dwaine Clarke, Univ. of the West Indies
Marten van Dijk, Univ. of Connecticut
Srinivas Devadas, Massachusetts Inst. of Tech.

2015 ACM TODAES Best Paper Award 2015

"A fast and scalable multidimensional multiple-choice knapsack heuristic"
Hamid Shojaei, *Univ. of Wisconsin*, Twan Basten, *Eindhoven Univ. of Tech.*, Marc Geilen, *Eindhoven Univ. of Tech.*, and Azadeh Davoodi, *Univ. of Wisconsin*,
Volume 18, Issue 4, Article 51, October 2013

Hamid Shojaei, *Univ. of Wisconsin*
Twan Basten, *Eindhoven Univ. of Tech.*
Marc Geilen, *Eindhoven Univ. of Tech.*
Azadeh Davoodi, *Univ. of Wisconsin*

ACM Outstanding New Faculty Award

In recognition of a junior faculty member who demonstrates outstanding potential as an educator and/or researcher in the field of electronic design automation.
Muhammad Shafique, *Karlsruhe Institute of Tech.*

ACM Outstanding PhD Dissertation Award

In recognition of an outstanding Ph.D. dissertation that makes the most substantial contribution to the theory and/or application in the field of electronic design automation.

Wenchao Li, *"Specification Mining: New Formalisms, Algorithms and Applications"*
Advisor: Sanjit Seshia, *Univ. of California, Berkeley*

ACM Fellows

To recognize and honor outstanding ACM members for their achievements in computer science and information Tech. and for their significant contributions to the mission of the ACM. In particular, we recognize the AMC Fellows involved in design automation research, including the areas of test, security, energy-efficient systems, embedded systems and SAT solvers.

Srinivas Devadas, *MIT*
For contributions to secure and energy-efficient hardware.

Nikil Dutt, *Univ. of California, Irvine*
For contributions to embedded architecture exploration, and service to electronic design automation and embedded system.

Shard Malik, *Princeton Univ.*
For contributions to efficient and capable SAT solvers, and accurate embedded software models.

Subhasish Mitra, *Stanford Univ.*
For contributions to the design and testing of robust computing systems.

Vijay Narayanan, *Pennsylvania State Univ.*
For contributions to power estimation and optimization in the design of power-aware systems.

Parthasarathy Ranganathan, *Google, Inc.*
For contributions to the areas of energy efficiency and server architectures.

Alberto Sangiovanni-Vincentelli, *Univ. of California, Berkeley*
For contributions to electronic design automation.

52nd DAC Best Paper Candidates

Six papers were nominated by the Technical Program Committee as DAC Best Paper Candidates. Final decisions will be made after the papers are presented at the Conference.

Research

14.1 An EDA Framework for Large Scale Hybrid Neuromorphic Computing Systems

26.1 DERA: Yet Another Differential Fault Attack on Cryptographic Devices Based on Error Rate Analysis

27.1 Battery Lifetime-Aware Automotive Climate Control for Electric Vehicles

30.1 Trends in Functional Verification: A 2014 Industry Study

32.6 Code Coverage of Assertions Using RTL Source Code Analysis

35.1 A Control-Theoretic Approach for Energy Efficient CPU-GPU Subsystem in Mobile Platforms

39.1 HAFIX: Hardware-Assisted Flow Integrity Extension

IP Track

1.4 Techniques for Power and IR Drop Optimization in Sensor Digital IP

15.3 Why Testbench Should Control Processor Execution: “A Novel Approach to Bridge the Gap Between IP and SoC Verification”

Designer Track – Back-End

6.3 A Methodology to Analyze Edge-to-Edge Jitter for High Speed DDR Interfaces with PDN Noise

6.5 Design Methodology for Operating in Near-Threshold-Computing (NTC) Region

38.2 Next Generation Hybrid Clock Tree

38.4 Accelerating Productivity Using Design Automation for Low Skew Global Clock Distribution in a Complex SoC

Designer Track – Embedded Systems and Software

9.2 Modeling Streaming Interfaces with Adaptive Accuracy Using TLM2

9.6 Architectural Exploration Platform for Solid State Drive Designs

44.2 Continuous Integration Build and Release Ingredients

44.5 System Simulator for High-Speed Link Design

Designer Track – Front-End

25.2 SAE-Platform: A Platform for System Architecture Exploration

25.6 Automatic Generation & Integration Of Test Management Structure at SoC Level Using IP-XACT Methodology

52.2 RTL2RTL Formal Equivalence: Boosting the Design Confidence

52.5 Hierarchical Lint with Abstract Models: An Efficient, Practical and Scalable Flow for Billion Gate SoCs

REVIEWERS

A total of 804 manuscripts were submitted to the 52nd DAC. The Technical Program Committee, together with the help of invited expert and external reviewers, selected 162 papers for presentation at the conference. The Conference Executive and Technical Program Committees wish to acknowledge the time and effort spent by the following people who reviewed these manuscripts. Many thanks to all of those who participated and contributed to the success of the conference.

Expert Reviewers (Topic experts invited by the TPC Subcommittee Chairs)

David Abercrombie - Mentor Graphics Corp.
Andrea Acquaviva - Politecnico di Torino
Allon Adir - IBM Research - Haifa
Giovanni Agosta - Politecnico di Milano
Subidh Ali - New York Univ.
Jason Allred - Hill Air Force Base
Sidharta Andalam - TUM CREATE Ltd.
Hugo Andrade - National Instruments Corp.
Christoph Angerer - NVIDIA
Andreea Simona Anghel - IBM Research
Saif Ansary - Virginia Tech
Eli Arbel - IBM Research - Haifa
Frederik Armknecht - Univ. of Mannheim
Amir Ashouri - Politecnico di Milano
Guillaume Aupy - École normale supérieure de Lyon
Rachata Ausavarungnirun - Carnegie Mellon Univ.
Philip Axer - Braunschweig Univ. of Tech.
Gasser Ayad - Politecnico di Torino
Aydin Aysu - Virgina Tech
Andrey Ayupov - Intel Corp.
Mainak Banga - Intel Corp.
Fang Bao - Qualcomm, Inc.
Antonio Barbalace - Virginia Tech
Alessandro Barenghi - Politecnico di Milano
Abhishek Basak - Case Western Reserve Univ.
Prabal Basu - Utah State Univ.
Debapriya Basu Roy - Indian Institute of Tech. Kharagpur
Vagelis Bebelis - INRIA
Andreas Becher - Univ. of Erlangen-Nuremberg
Peter Beerel - Univ. of Southern California
Giovanni Beltrame - École Polytechnique
Amitava Bhaduri - Intel Corp.
Sharath Bhat - Virginia Tech
Alberto Bocca - Politecnico di Torino
Santiago Bock - Univ. of Pittsburgh
Srinivas Boppu - Univ. of Erlangen-Nuremberg
Amirali Boroumand - Carnegie Mellon Univ.
Adnan Bouakaz - INRIA
Youcef Bouchebaba - Synopsys, Inc.
Tobias Bund - Ulm Univ.
Steven Burns - Intel Corp.
Andrea Calimera - Politecnico di Torino
Rosario Cammarota - Qualcomm, Inc.
Arquimedes Canedo - Siemens Corp.
Vito Giovanni Castellana - Pacific Northwest National Laboratory
Rajat Subhra Chakraborty - Indian Institute of Tech. Kharagpur
Koushik Chakraborty - Utah State Univ.
Saumya Chandra - Advanced Micro Devices
Kevin Chang - Carnegie Mellon Univ.
Chip Hong Chang - Nanyang Technological Univ.
Chia-Ling Chang - National Chao-Tung Univ.
Tam Chantem - Utah State Univ.

Anupam Chattopadhyay - Nanyang Technological Univ.
Wenjie Che - Univ. of New Mexico
Mingsong Chen - East China Normal Univ.
Wen Chen - Freescale Semiconductor, Inc.
Yi-Jung Chen - National Che Nan Univevrsity
Andy Chen - National Tsing-Hua Univ.
Ke Chen - Oracle Corp.
Yukai Chen - Politecnico di Torino
Bo Chen - Portland State Univ.
Yuankai Chen - Synopsys, Inc.
Hu Chen - Utah State Univ.
Ron Chiang - Univ. of St. Thomas
David Chinnery - Mentor Graphics Corp.
Jongmoo Choi - Dankook Univ.
Wonje Choi - Washington State Univ.
Kai Cong - Portland State Univ.
Aijiao Cui - Harbin Institute of Tech.
Tamer Dallou - Technical Univ. of Berlin
Anup Das - Univ. of Southampton
Sourav Das - Washington State Univ.
Julien Deantoni - Univ. Nice
Yixiao Ding - Iowa State Univ.
Duo Ding - Oracle Corp.
Shai Doron - IBM Research - Haifa
Silvio Dragone - IBM Research
Michael Drescher - Virginia Tech
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Karthi Duraisamy - Washington State Univ.
Stephan Eggersglüß - Univ. of Bremen
Begum Egilmez - Northwestern Univ.
Mohammed El-Shambakey - Virginia Tech
Ylies Falcone - Univeristy Grenoble Alpes
Joachim Falk - Univ. of Erlangen-Nuremberg
Shao-Yun Fang - National Taiwan Univ. of Science and Tech.
Farimah Farhamandi - Univ. of Florida
Leandro Fiorin - IBM Research
Eric Foreman - IBM Corp.
Nicolas Fournel - Université de Grenoble-Alpes
Simeon Furrer - IBM Research
Davide Gadioli - Politecnico di Milano
Raviv Gal - IBM Research - Haifa
Deepak Gangadharan - Univ. of Erlangen-Nuremberg
Ping Gao - Aries Design Automation
Jhih-Rong Gao - Cadence Design Systems, Inc.
Saugata Ghose - Carnegie Mellon Univ.
Heiner Giefers - IBM Research
John Gilchrist - Mentor Graphics Corp.
Michael Glass - Univ. of Erlangen-Nuremberg
Ali Gok - Northwestern Univ.
Gilbert Goodwill - Cryptography Research
Dhananjay Griyage - Mentor Graphics Corp.
Warren Gross - McGill Univ.
Artjom Grudnitsky - Karlsruhe Institute of Tech.
Xiaofei Guo - Intel Corp.
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