COMPUTER ARCHITECTURE NEWS

A Quarterly Publication of the
Special Interest Committee
on Computer Architecture

Contents:

January 1972, Volume 1, Number 1

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ACM Special Interest Committee on
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COMPUTER ARCHITECTURE NEWS is an informal quarterly publication of the ACM Special Interest Committee on Computer Architecture (SICARCH) whose scope of interest included all phases of the design, organization and structure of computing systems.

Membership in SICARCH is open to all who wish to belong.

Contributions to CAN should be sent to the editor, and should not ordinarily exceed 1000 words, and should be single-spaced with 1 inch margins in camera-ready form. All letters to the editor will be considered for publication unless accompanied by a request to the contrary. Except for editorial items, all sources of material appearing in Computer Architecture News will be clearly identified. Items attributed to individuals will ordinarily be interpreted as personal rather than organizational opinions.

Technical papers appearing in this issue are unrefereed working papers except where indicated.

SICARCH FORMED

At the ACM council meeting in Chicago, August, 1971, the Special Interest Committee on Computer Architecture was formed. Chairman of the new group is Michael Flynn, vice chairman is Caxton Foster and secretary-treasurer is Conrad Wogrin. The area of interest of this group lies somewheres between the fields of logical design and operating systems with considerable overlap at each end. Primary emphasis will lie in the design and construction of "computing systems" with all that that entails.

This newsletter will be issued quarterly in January, April, July and October. It will contain the usual notices of coming events that may be of interest to its readers. Every attempt will be made to keep these to notices about future events rather than historical notes. In addition, we will include letters from members expressing a point of view or requesting information. Further, we will publish short notes on architectural topics as they are received. Since this is an unrefereed newsletter these notes do not constitute "publication" in the academic sense and may be submitted elsewhere. Unfortunately, the U.S. Patent Office takes the attitude that printing here is "publication" in their sense and, hence, one has only a year following such printing to apply for a patent. Finally, we hope to include abstracts of current literature. Anyone with a bibliography on some aspect of computer architecture is hereby urged to share it with our readers. Discussions of various machine designs will be welcome but PR releases will not. A series of notes on older (and, possibly, newer) machines - their salient features, good and bad- would be very useful for those of us who did not have direct experience with them.

CHAIRMAN'S REPORT

Computer Science
The Johns Hopkins University
Baltimore, Maryland 21218

December 13, 1971

Dear Friends and Colleagues:

With this newsletter, a new SIC is launched; hopefully to serve the genuine interests of computer designers and programmers with interest in computer organization. Only your interest, help and cooperation over the next year will make SICARCH viable and allow us to become a SIG. It is our plan to be in close cooperation with our sister operation (the IEEE Computer Society, Technical Committee on Computer Architecture) so as to avoid needless duplication, yet to make the work of people interested in computer design available to members of both IEEE and ACM. It is our hope to run joint meetings, jointly sponsored symposia, etc. Personally, I feel that opening membership in virtually a single professional organization (to both IEEE and ACM members) a great deal is gained. However, I must share with you that I have underestimated the amount of administrative difficulties involved.

This issue of the newsletter will also go to all former members of SIGREAL. SIGREAL recently disbanded. A number of its members indicated their desire to transfer to SICARCH. This newsletter is an open invitation to all SIGREAL members to join in making SICARCH a success. There is no cost for a SIGREAL member to convert his membership to SICARCH, but in order to have this happen and continue to receive this newsletter, the SIGREAL member must fill out the attached form and send it to ACM headquarters.

The interest of all members in the newsletter and the workshops, which we will be sponsoring, will make SICARCH a success.

Mike Flynn

Michael J. Flynn

DATES OF INTEREST

Spring Joint Computer Conference - Atlantic City - May 16-18, 1972

Contact: AFIPS
210 Summit Avenue
Montvale, New Jersey 07645

Workshop on Parallel Computation - Seattle - June 20-22, 1972

A call for abstracts has been issued for the Workshop on Parallel Computation, to be held June 20-22, 1972 under the joint sponsorship of the Technical Committee on Computer Architecture of the IEEE Computer Society, and SICARCH of the Association for Computing Machinery. Papers and abstracts on all phases of parallel computation are welcome including such areas as:

machine architecture including pipeline machines, array processors, and multi-processors
parallel algorithms
large scale computations
system implementation including data management, scheduling, and resource allocation
performance evaluation
programming languages

Prospective speakers are asked to submit an abstract or digest of at least 300 words to the program chairman, Dr. Richard Wishner, Systems Control, Inc., 260 Sheridan Avenue, Palo Alto, California 94306, by March 1, 1972. For information other than submission of the program, contact the arrangements chairman, Professor Jean-Loup Baer, Computer Science Group, University of Washington, Seattle, Washington, 98105.

ACM 1972 - Boston, August 14-16, 1972

We have been approached about supporting the ACM annual conference to be held in Boston in August, 1972. SICARCH has agreed to run a tutorial session with a working title "What's New In Computer Architecture". This is to be organized by Mr. James Pomerene of the IBM Corporation, Armonk, New York. Professor Richard Eckhouse of the Computer Science Department, University of Massachusetts, Amherst, Massachusetts 01002 has agreed to organize a session for contributed papers in the area of computer organization.

COMPCOM 72 - San Francisco, September 12-14, 1972

The next IEEE Computer Society Confrence will be held in San Francisco, September 12-14, 1972. Its theme is "Current Achievements and New Directions in Computer Systems Design". This conference will stress Computer Architecture and will publish short digests of each presentation. A presentation of a paper at this conference does not preclude publication of the full contribution elsewhere. Several of the areas of solicitation of the program included:

1. Computer Systems of increasing complexity (including operation arrays, parallel processors, and hardware implemented operating systems and higher level languages).
2. Measures of Computer Performance (including modeling, analysis of systems, as well as, general techniques).
3. Functional Parts of a Computer System (arithmetic algorithms, storage hierarchies, microprogramming).
4. Tools for System Design (simulators, etc.)
5. The influence of related disciplines on computer systems architecture.

6. Case studies of current computer systems.

A number of TCCA members have already agreed to assist in the organization of sessions for COMPCOM 72:

1. Harvey Garner - Computer Arithmetic
2. Dick Aschenbrenner - Techniques of Performance Evaluation
3. Harold Stone - Parallel Processors
4. Robert Ellis - Modular Computers

Suggestions, questions, and comments should be directed to the Program Chairman:

Professor A. Avizienis
UCLA Computer Center
Department BH3732
University of California
Los Angeles, California 90024

Papers should be received by May 1, 1972.

Arithmetic Workshop - College Park, Maryland, May 15-16, 1972

This workshop is to be held at College Park, Maryland on May 15-16, 1972 with transportation to Atlantic City for the SJCC being provided by the workshop. The IEEE is the primary sponsor of this, however, the ACM has been requested to provide a cooperating sponsorship.

Prospective authors please notify intention to submit papers as soon as possible to the Program Chairman:

Professor Daniel Atkins
Computing Center
Bucknell University
Lewisburg, Pennsylvania
17837

Papers are solicited in the areas of: Theory of Arithmetic, Arithmetic Codes, Number Systems, Arithmetic Algorithms and Implementation, Precision and Conversion, Error Control and Specific Arithmetic Subsystems. Authors must submit an abstract (of not more than 200 words) and a draft of the paper for review by March 1, 1972 to Professor Atkins. For further information, you may contact:

Symposium Chairman:	Professor H. L. Garner University of Pennsylvania Philadelphia, Pennsylvania
Local Arrangements Chairman:	Professor T. R. N. Rao University of Maryland College Park, Maryland
Publicity Chairman:	Professor O. N. Garcia South Florida University Tampa, Florida

PROPOSED DEFINITION OF COMPUTER ARCHITECTURE

Professor Yaohan Chu of the University of Maryland, College Park, Maryland has proposed a definition of computer architecture. Your comments and alternative proposals are welcome and will be printed in future issues. Professor Chu says:

> "Computer Architecture is an emerging discipline as a result of recent rapid technical advances in computer technology. Instead of merely studying the hardware structural and algorithmic features of a computer system, the scope of computer architecture is being broadened to the conceptual formation and specification of computer systems. Full recognition of and formal training in computer architecture will hasten computer applications to new horizons. Before the end of this decade, a new breed of professionals, computer architects, will arise. Computer architects practice computer architecture just as building architects practice building architecture."

THE STANDARDS REPRESENTATIVE

Both IEEE and ACM have approached us for a standards representative, that is, someone who could review proposals and update some existing standard definition of terms. Professor Alan Marcovitz of Florida Atlantic University graciously accepted the nomination as Standards Representative to both IEEE and ACM. His address is:

Professor Alan B. Marcovitz, Chairman
Department of Electrical Engineering
Florida Atlantic University
Boca Raton, Florida 33432

ARITHMETIC STANDARD

In line with the above there was discussion at the SICARCH/TCCA meeting in Las Vegas of an arithmetic standard proposed by Mr. M. Perstein of the System Development Corporation and addressed to ANSI/X3. The proposal was quite detailed in scope, specifying sign and magnitude representation ("for all numbers") radix 2 for floating point numbers, and included general specifications for the relative size of the fraction, location of the sign, exponent and fraction and rather detailed specifications of the jump instructions. After considerable discussion, a resolution was passed:

> "It is resolved that this kind of standardization is overly restrictive and, hence, detrimental to good design practice. Further, any arithmetic standard should specify operational criteria and definitions rather than design details. Further, SICARCH and TCCA would be responsive to cooperate in work in this area, if desired."

(Editor's note: I wasn't at the meeting so, perhaps, I shouldn't make any comments but I will anyway. It seems to me that it is the responsibility of those who reject a proposed standard to do so only after having come up with another (hopefully, better) proposal to substitute for the rejected one. That way, we approach by small but finite steps the presumably desirable state of having standards about things. God did not decree, or even recommend highly, one's complement, two's complement, or sign and magnitude. So let's pick one of them, any one will do, standardize on that and get on with the job in hand. Resolutions like this one are of the "all possible assistance short of actual help" type. Their major function is to turn off people who might want to suggest standards. May we have some reader comments on this?)

PAPERS OF INTEREST

Fred F. Coury, A Systems Approach to Minicomputer I/O, SJCC, 1970, pp. 677-681.

- A provocative examination of what effect there might be if CPU prices went to zero. Some good systems philosophy.

Wallace B. Riley, Wanted for the '70s: Easier-to-program Computers Electronics, September 13, 1971, pp. 61-84.

- What our hardware brethern think is ahead in the next decade. Well written and speculative. Read it.

Donald E. Knuth, An Empirical Study of FORTRAN Programs, Software-Practice and Experience, Vol. 1, pp. 105-133 (1971).

- This article tells you a great deal about how programmers use computers. Don't you think it might be nice to know that before you design your next machine?

ARCHITECTS SKETCH PAD

This section will consist of short notes describing ideas that seem to be of possible interest to computer architects. This issue, both notes, are by your editor. If our readers will submit ideas, we will be most happy to publish them. This is not intended to be a private soap-box.

Hardware Control for Gated Entry

Multics has a ring structure for controlled entry to system segments. Would the following technique help them or others?

Suppose a paged environment. Let each segment begin at the beginning of a new page. Jumps (conditional or unconditional) within a page will function as before but when an address is loaded into the program counter, that is out of the current page, the desired address is loaded into the PC as on an in-page jump but what gets sent to the MAR for the I-fetch is the address of line zero of the new page. We suppress transfer of the low order bits. If the first instruction of the destination page is a NOP, then the next instruction fetched will be from the line pointed at by the PC. Namely, the one the programmer specified. If, however, the first instruction in the new page is a JMP *+1, we have completely controlled entry and can do validity checks etc. right in the segment in question withour generating an interrupt or bothering the operating system in any way. Cost should be very low. Anybody think it might be useful? Does it want a defeat switch for multipage segments or not?

--- Caxton Foster

Symmetry of Addressing Modes

For years, it has bothered me that there is no normally recognized "inverse" to an "enter accumulator with the address field" - an immediate load instruction. That is, "desposit accumulator immediate" doesn't exist. After a good deal of thought, I would like to propose the following four modes of addressing. I do not propose that they be built into the hardware, just that we recognize that they exist. Consider a two address instruction with one source and one destination. MOV α, β which copies the contents of α into β in the PDP-11 is an excellent example.

Mode 0, Symbolic When applied to the source, mode 0 specifies the bit string which corresponds to the symbol "α". If α is the letter "A" and ASCII is the internal code, then MOV 0 A,β will put the byte: "11000001_2" into β. When applied to the destination, mode 0 "defines" the bit string which will be used to represent the symbol β. If location α contains the bit string "11000010_2" then MOV α, 0 B will made the bit string "stand for" the letter B. Normally this definition of the bit strings is done at "machine design time" but it is well to remember that it is done sometime.

Mode 1, Locative When applied to the source, mode 1 specifies the address which has been assigned to the name "α". If variable SMITH has been assigned to storage address 1234 than MOV 1 SMITH, α puts 1234 into α. Note that many assemblers blur the distinction between mode 1 and mode 0 when applied to sources. When applied to a destination, mode 1 assigns the value of the source to be the address of the name given as the destination. If α contains the number 1234 then MOV α,1 SMITH assigns

to the variable SMITH a storage address of 1234. This is called "building the symbol table" and is a well recognized function of assemblers and compilers. We propose making it an executable instruction, perhaps, via a macro or microprogramming.

Mode 2, Dative This is the "normal" direct addressing. MOVE 2 JONES, 2 BROWN takes a copy of the contents of variable JONES (the current value of JONES) and uses that to replace the contents of variable BROWN.

Mode 3, Nominative This is normal "indirect" addressing. MOV 3 BLUE, 3 GREEN - the contents of the cell whose address is stored in the source (BLUE) is used to replace the contents of the cell whose address is stored in the destination (GREEN).

To state this all a different way:

mode	meaning
0	- the symbol itself
1	- contents of the symbol table entry = C(STE)
2	- contents of the contents of the symbol table entry = C(C(STE)).
3	- contents of the contents of the contents of the symbol table entry = C(C(C(STE))).

When applied to a source, this means "use the thing specified as the value to be moved". When applied to a destination, we mean "replace the thing specified by the value of the source".

--- Caxton Foster

Closing Comments

Please feel encouraged to participate in this newsletter anyway you would like. Letters to the editor, references, sketch pad notes, etc. will all be eagerly accepted. Comments, comments on comments, etc. recursively defined will be welcome. Unless you contribute to this newsletter, you will get nothing but Fosterisms and that may pall after a while.

--- C. C. F.

Please add the following names to the SICARCH mailing list:

_____	_____
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If a SIGREAL member and this is a transfer of membership

check here ☐

mail to: Membership Section of the ACM Inc.
1133 Avenue of the Americas
New York, New York 10036

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1133 Avenue of the Americas, New York, New York 10036